→ EMPIRE XPU

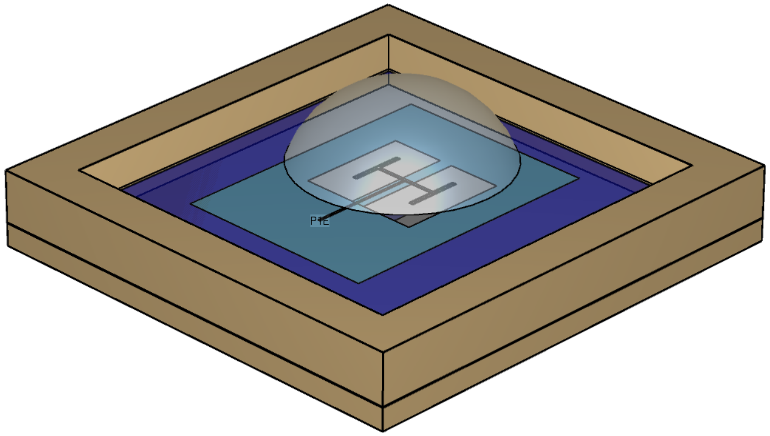
3D EM for RFIC

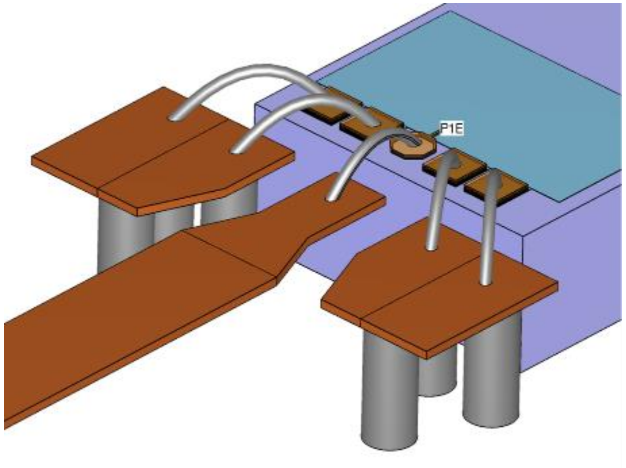
www.muehlhaus.com

Agenda

- ✓ Introduction: Why use Empire XPU?
- ✓ Basics: Using Empire (LIVE)
- ✓ Some RFIC examples (LIVE)
- ✓ Overview of App Notes

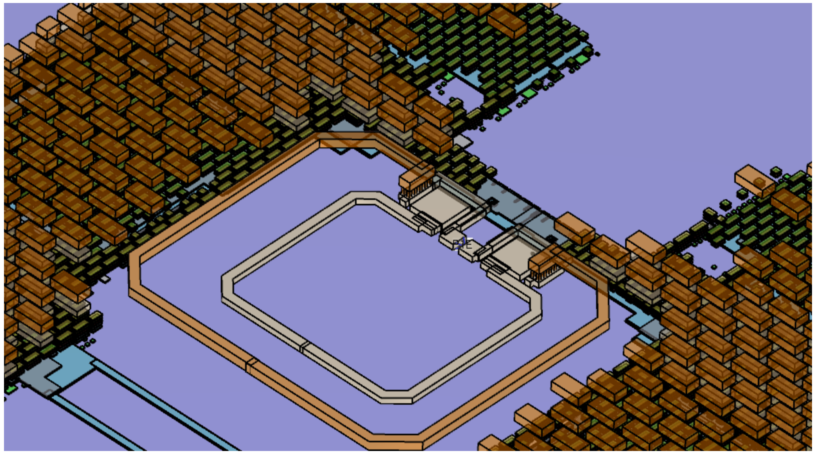
RFIC EM Simulation Challenges

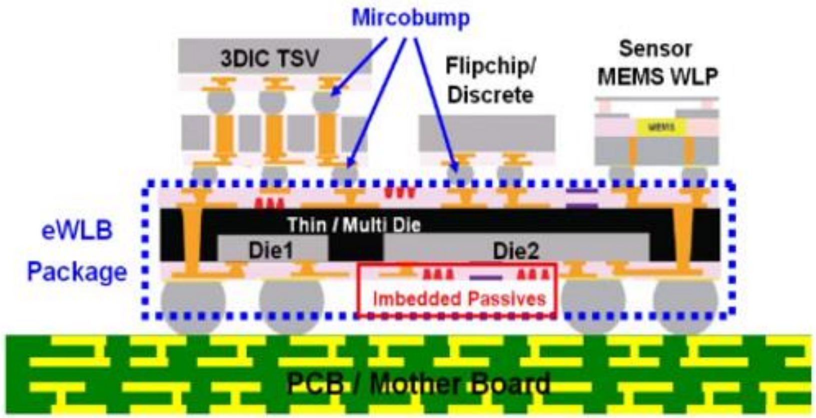




Combination of layered 2D design and 3D elements

Layout complexity – many objects



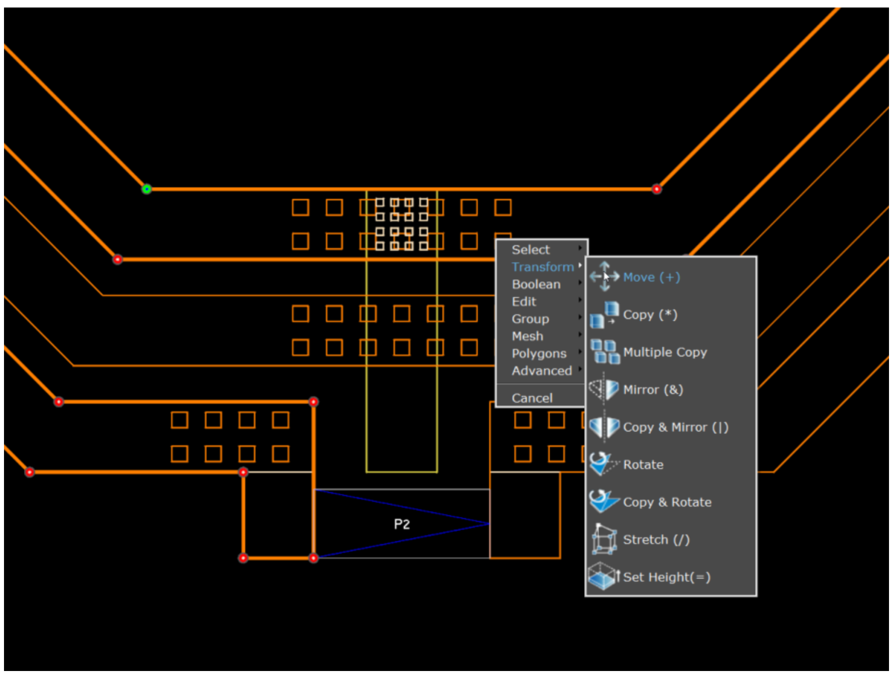


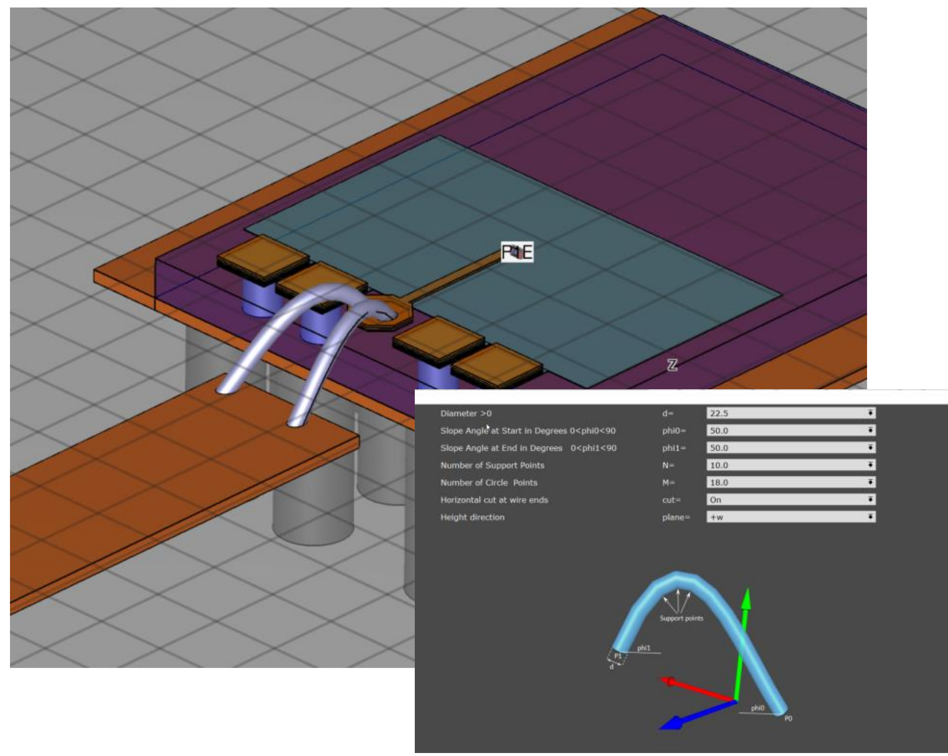
Why use Empire XPU?

- ✓ **Efficient modelling: User interface with 2D and 3D editor mode**
  ideal for layered structures with additional 3D elements
- ✓ **Objects grouped by "layers"**
  that provide z-position, materials, priorities, layer-specific mesh settings and much more.
- ✓ XPU FDTD solver can handle **very large, complex models**
- ✓ **Much faster** than other time domain solvers by using XPU technology
- ✓ **High simulation speed enables more detailed, more accurate models**

Edit your model in 2D and 3D

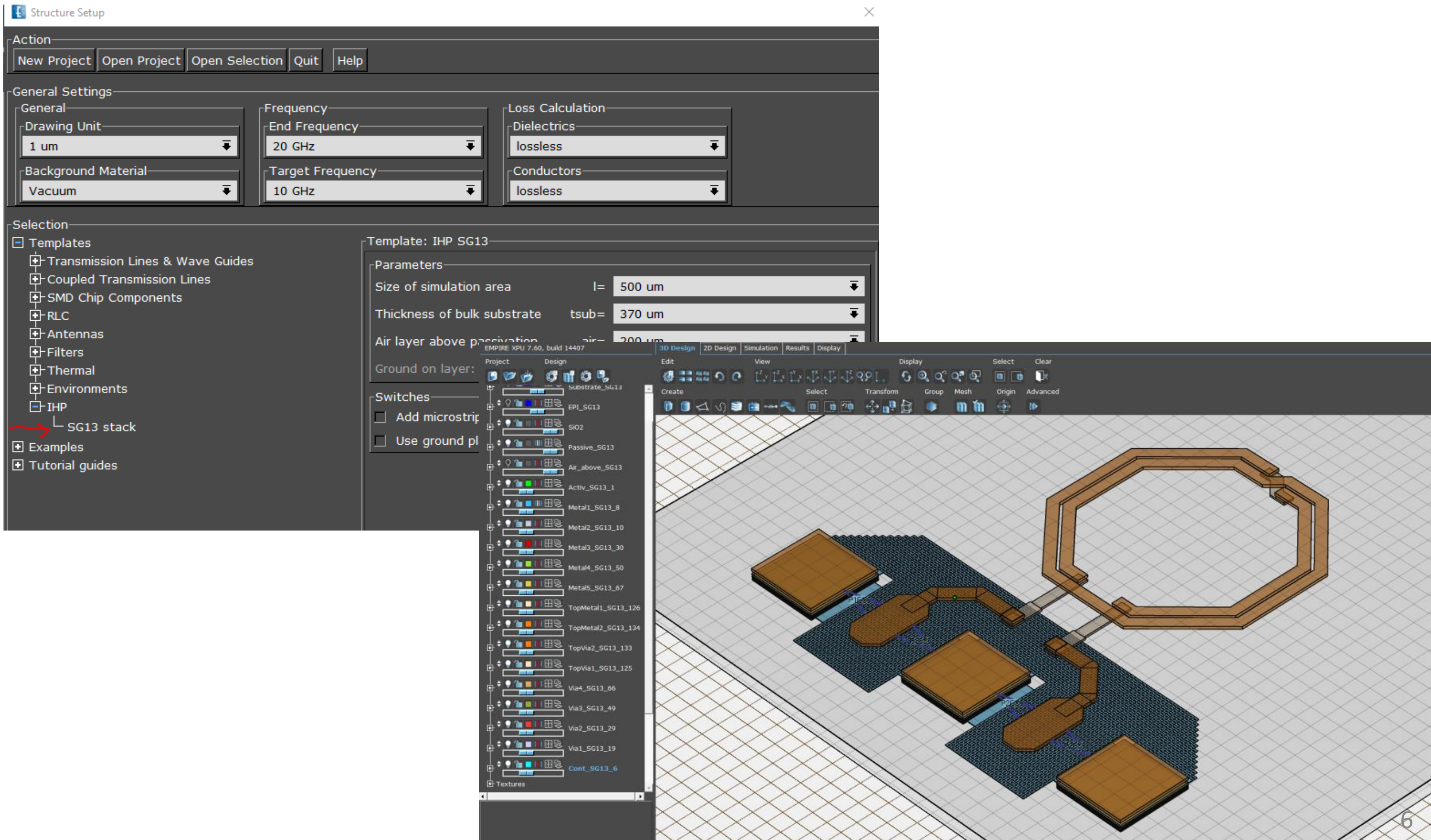
- ✓ 2D Design mode, optimized for multi-layered circuits and components, with full-featured 2D import & export capabilities
- ✓ 3D Design mode for general 3D structures with snap on grid and object surfaces
- ✓ Easily switch between 2D editor and 3D editor at any time
- ✓ Import existing models from CST & HFSS



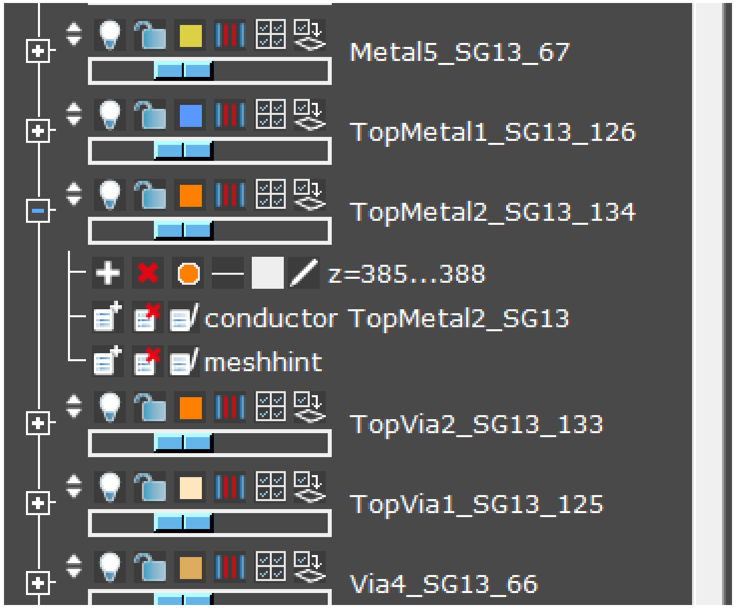


Build your model faster with Templates

- ✓ Templates for IHP technologies + layout from GDSII
- ✓ Templates can also preset mesh settings and loss model per layer



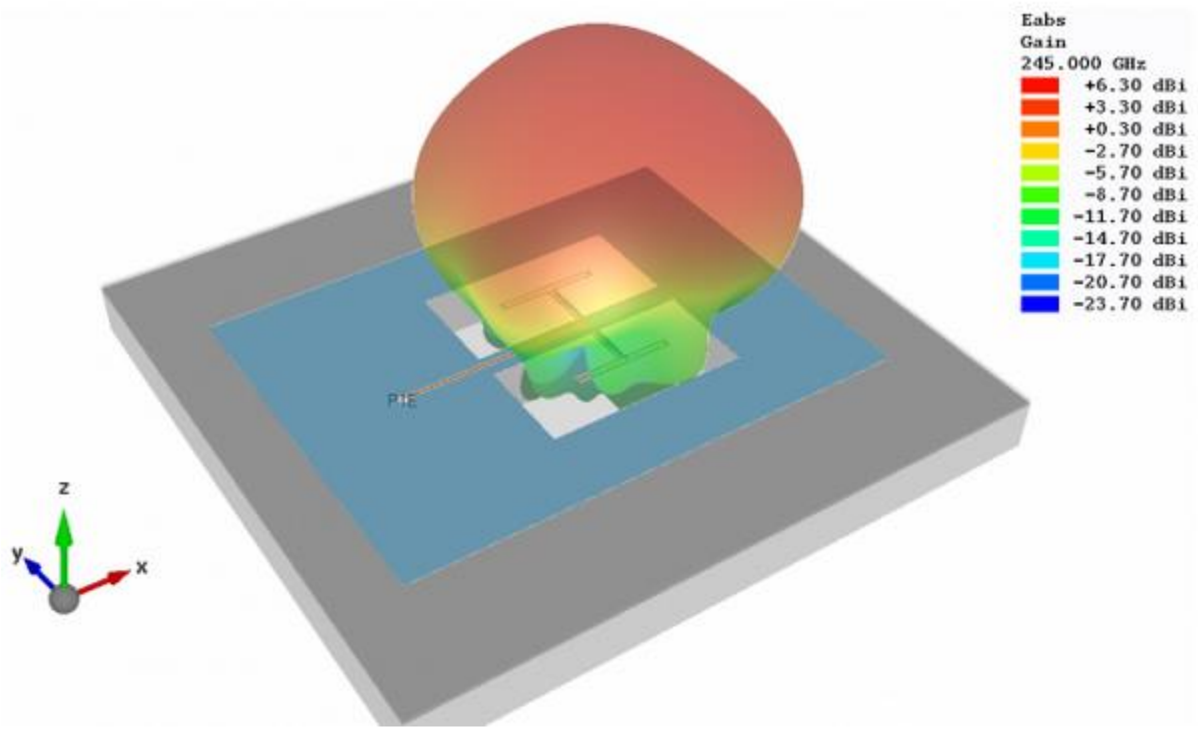
Layers: Much more than just layers



- ✓ Layer from template can provide:
  - default z-position and thickness
  - material properties
  - priority
  - layer-specific mesh control
- ✓ Layer values are default for objects on that layer. You can override values if needed.
- ✓ Priority defines which object "wins" for overlapping geometries.
  Example: LBE hole in substrate

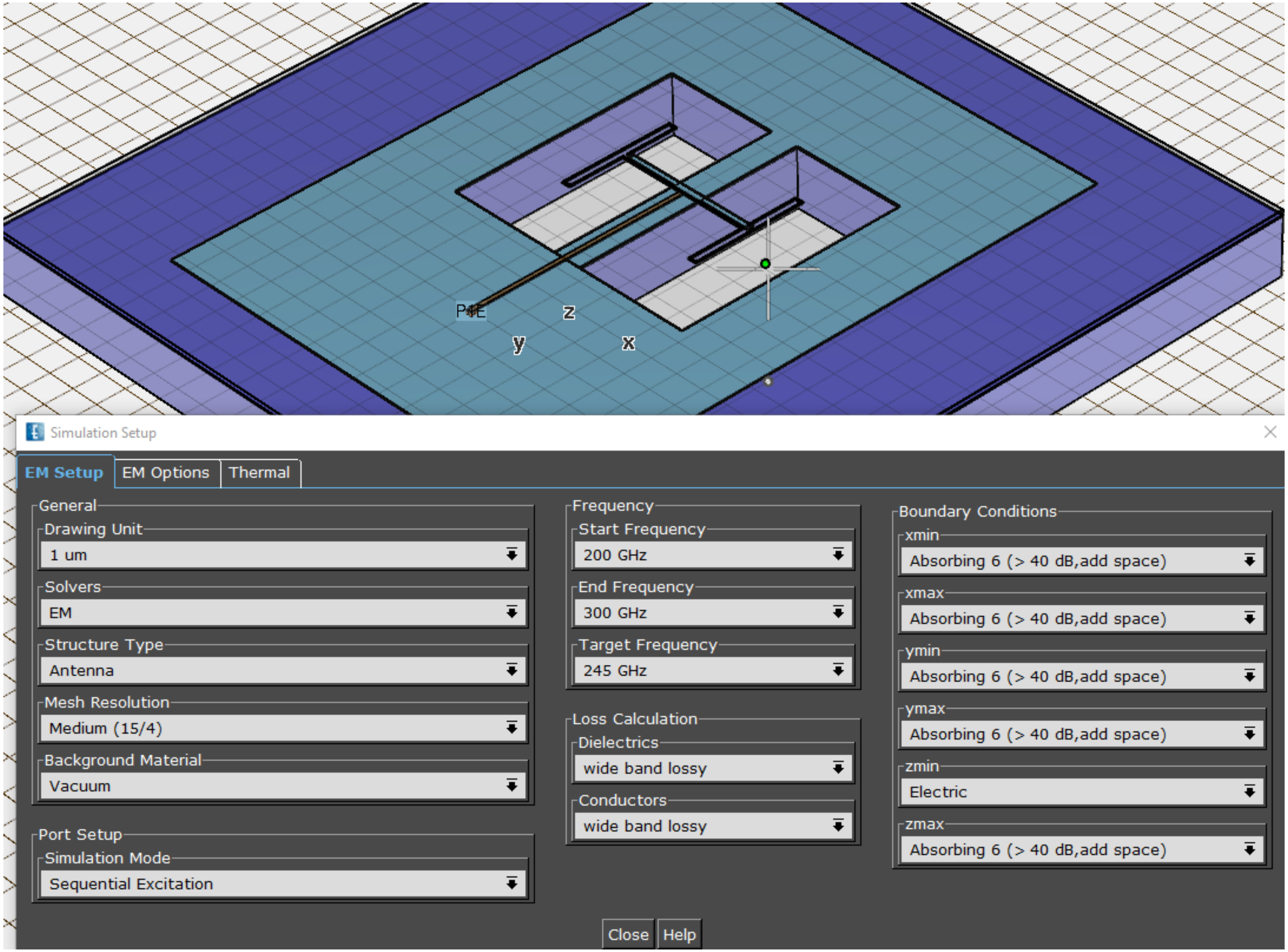
240 GHz Antenna in SG13S with Backside Etching

- Original design by IHP authors: *K. Schmalz, W. Ruoyu, J. Borngräber, W. Debski, W. Winkler , and C.Meliani, "245 GHz SiGe transmitter with integrated antenna and external PLL," in IEEE IMS, 2013, pp. 1–3.*

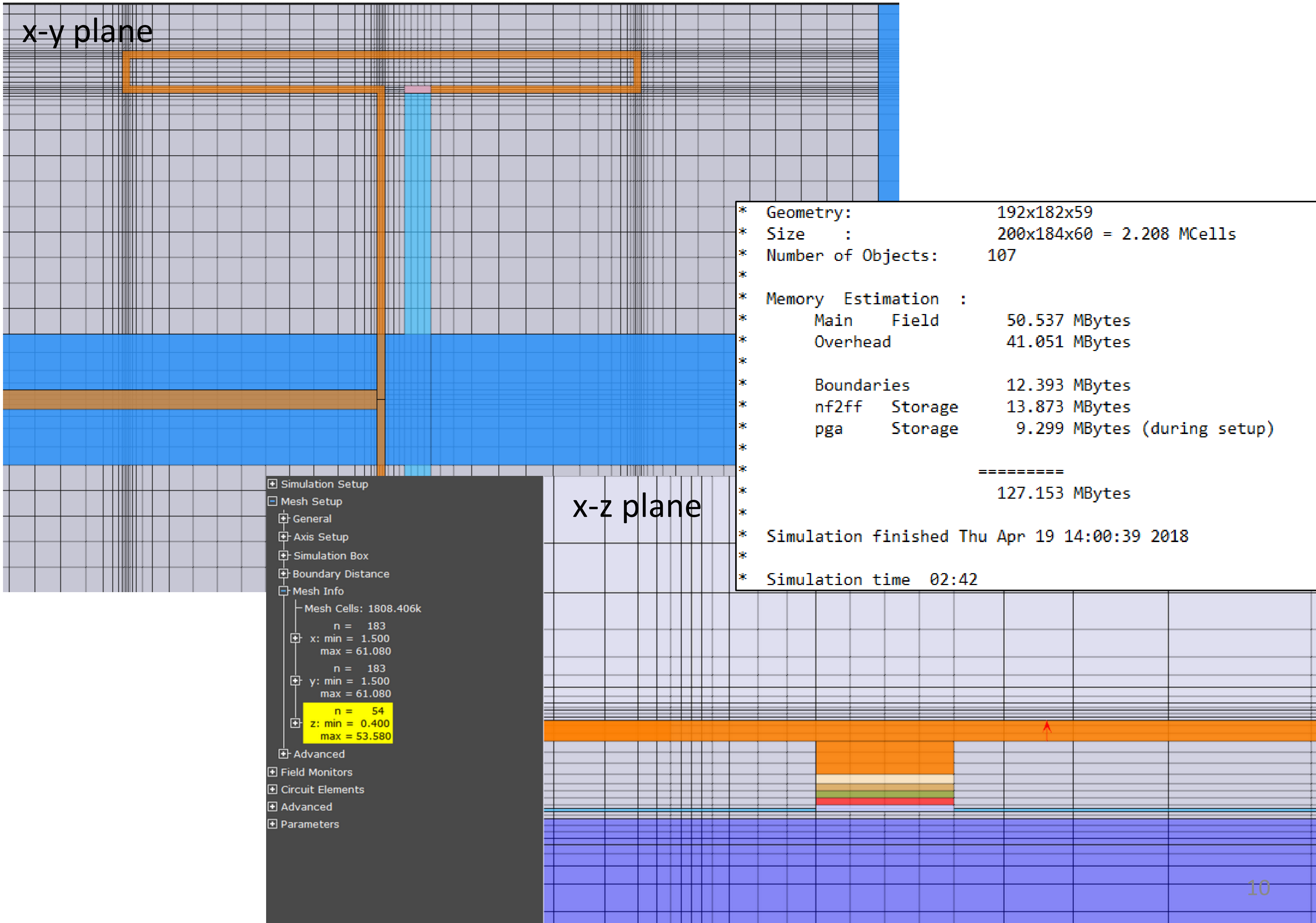


http://muehlhaus.com/support/empire-appnotes/empire-on-chip-antenna-240ghz

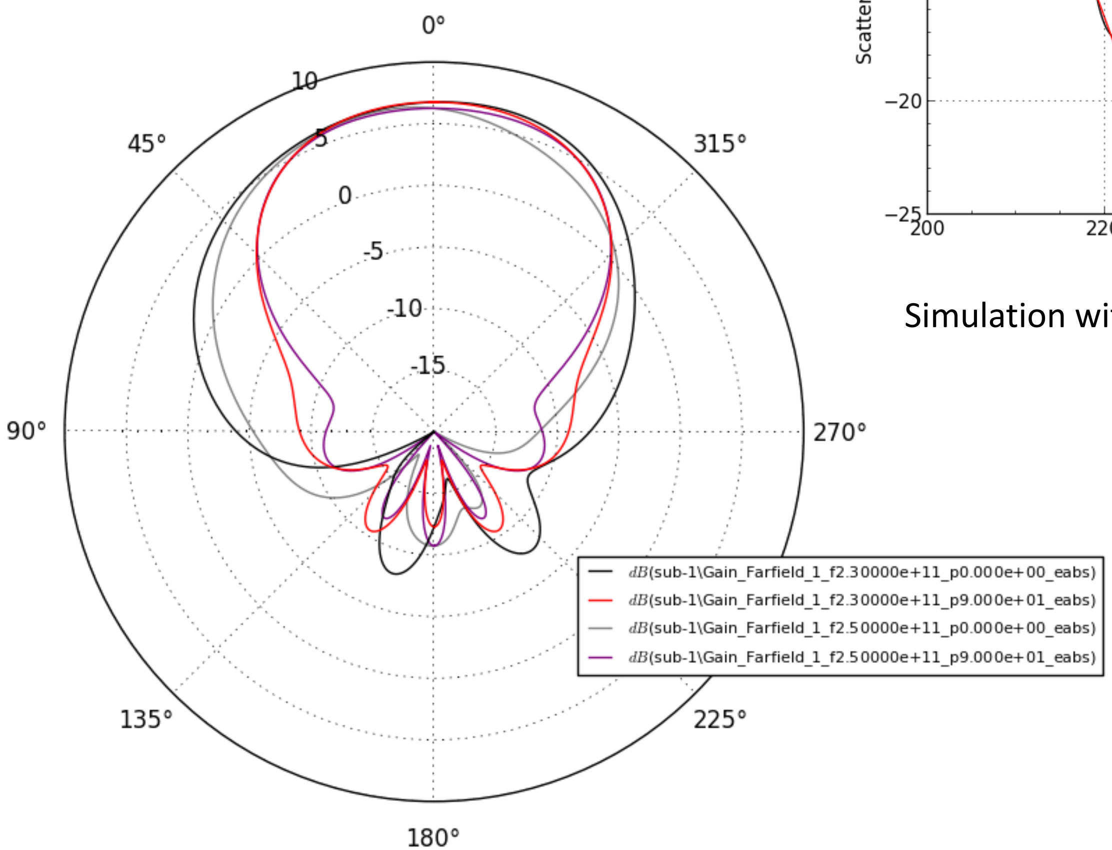
240 GHz Antenna

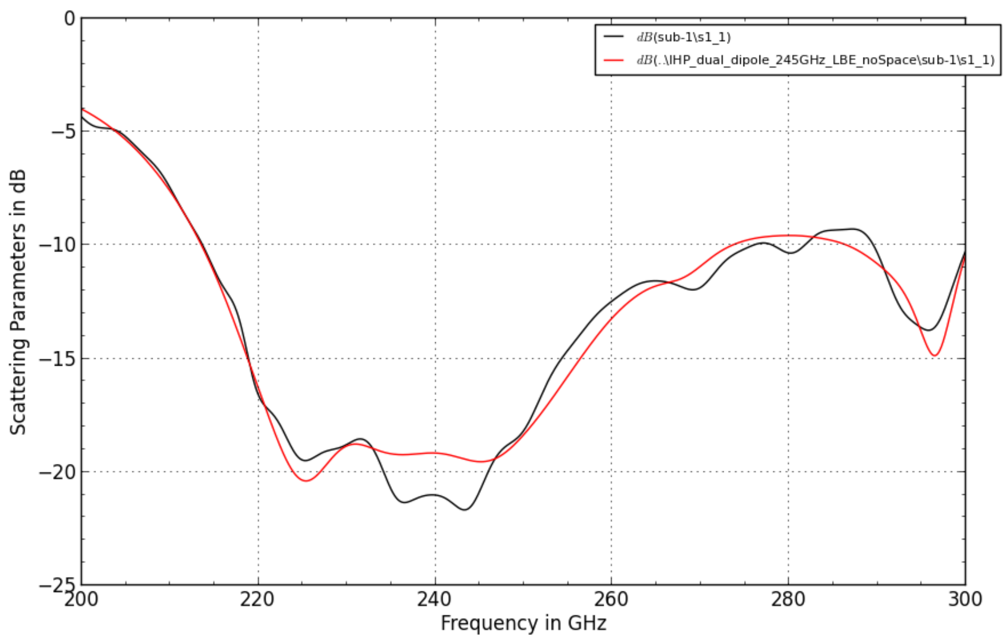


240 GHz Antenna - Mesh



240 GHz antenna – Simulation Results

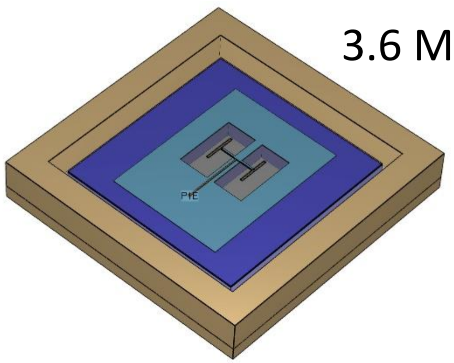




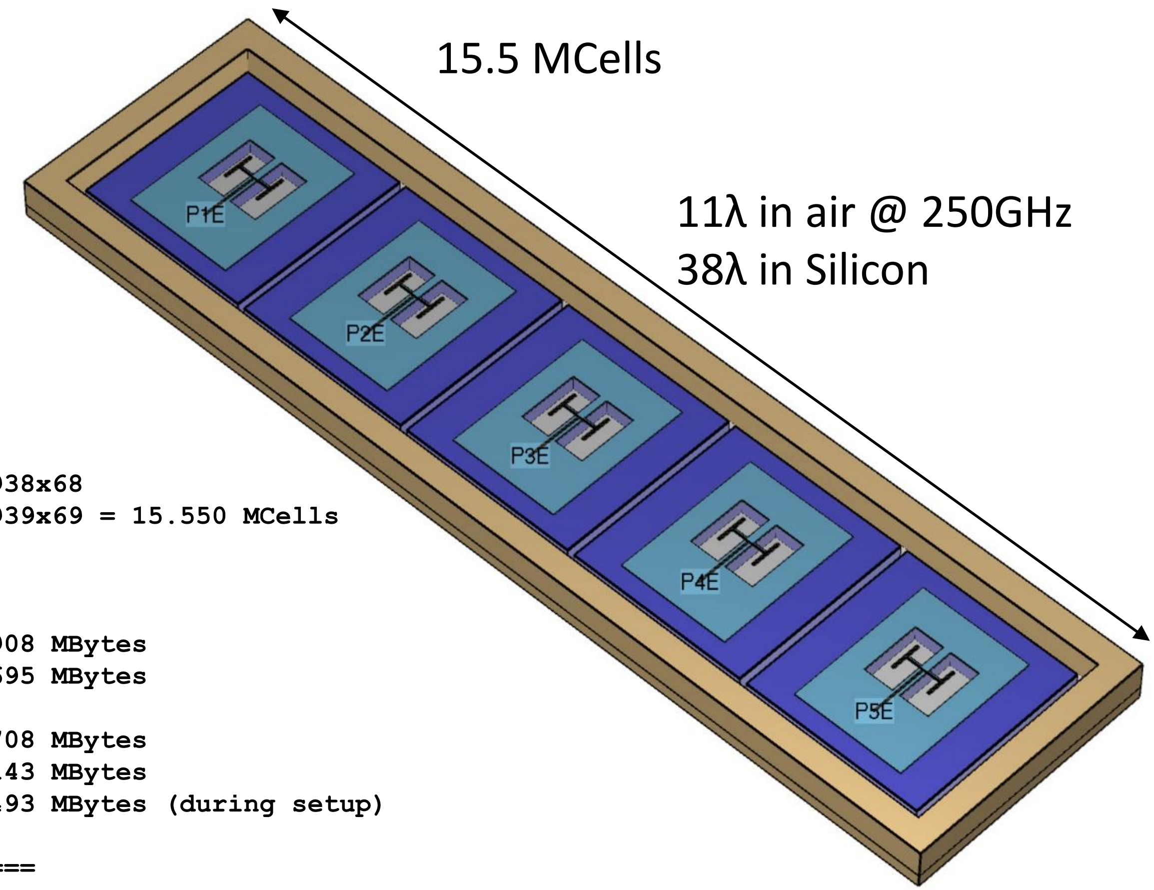
Simulation with 200µm substrate = 220µm total chip thickness

Go to larger models without hitting RAM limits

- ✓ FDTD method has less memory requirement than FEM or MoM when creating electrically large models
- ✓ Required RAM scales **linear** with number of mesh cells, enabling large models



3.6 MCells



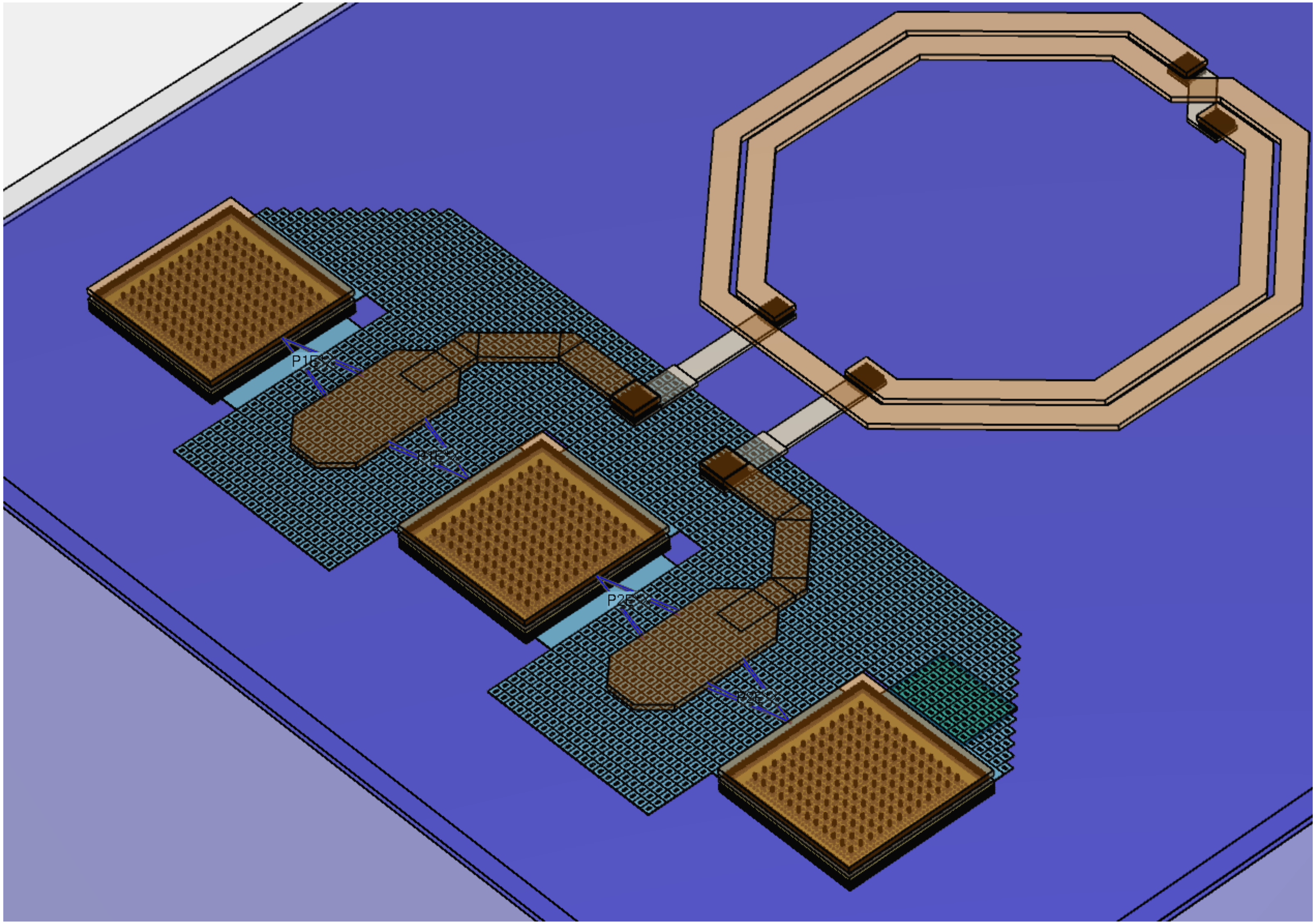
15.5 MCells

11λ in air @ 250GHz
38λ in Silicon

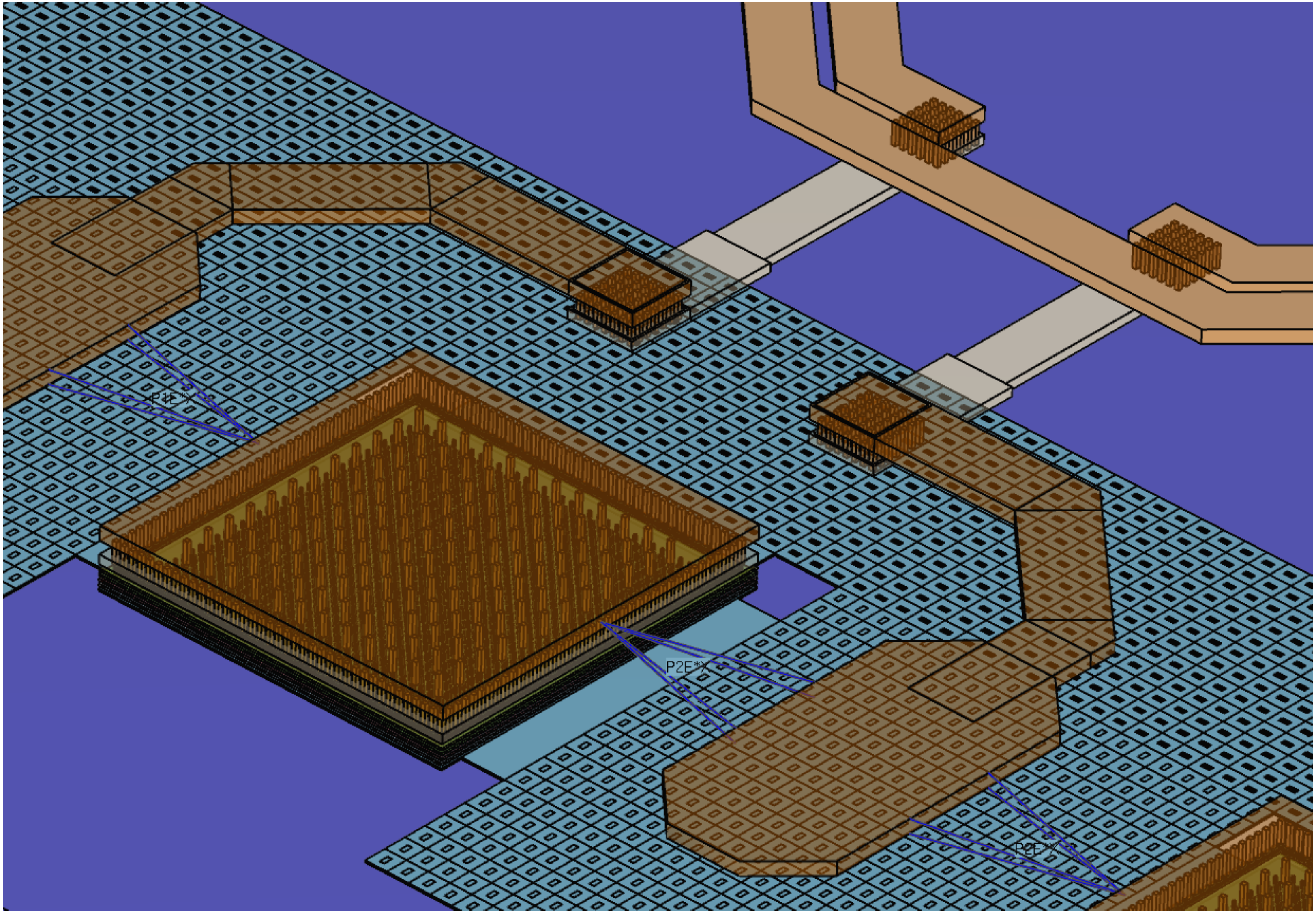
```
*   Geometry:                232x938x68
*   Size     :               240x939x69 = 15.550 MCells
*   Number of Objects:      427

*   Memory  Estimation   :
*        Main    Field       355.908 MBytes
*        Overhead             54.695 MBytes
*
*        Boundaries           57.708 MBytes
*        nf2ff   Storage      72.143 MBytes
*        pga     Storage      72.493 MBytes (during setup)
*
*                          =========
*                            612.947 MBytes
```

Large Model: All Via1 … TopVia2 without merging



Large Model: All Via1 … TopVia2 without merging

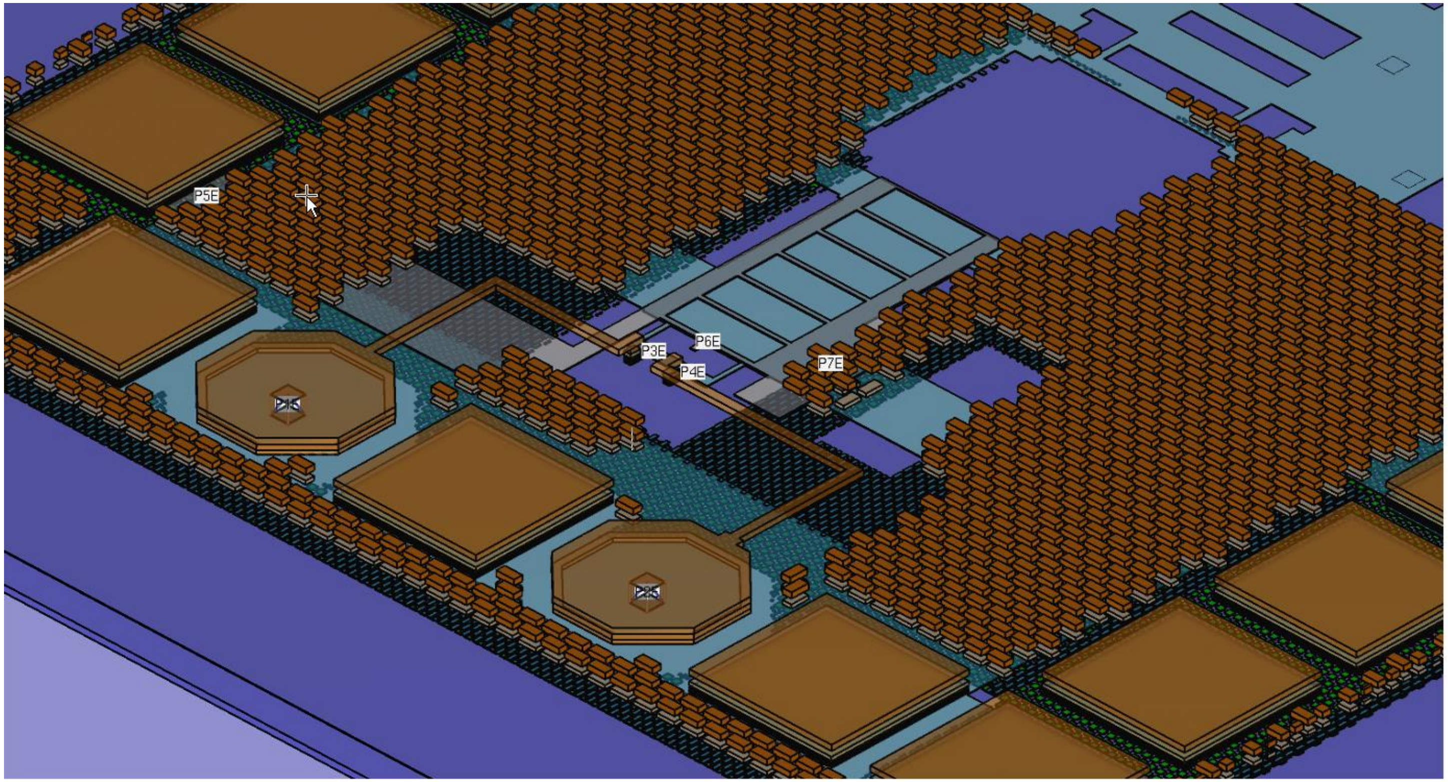


Large Model: All Via1 … TopVia2 without merging

- ✓ 2 Ports
- ✓ 95479 polygons, 51 million cells
- ✓ 3h:15min simulation time per port on Core i9-7940X
- ✓ Required memory: 2.5GB

```
*  Simulation Starting Thu Apr 26 18:28:23 2018
*  Using AVX+FMA3 vectorisation Extension in 1 cpu groups, 14 cores alltogether
*
*  Geometry w/o abc:       609x1204x67
*  Geometry:               611x1206x68
*  Size    :               616x1208x69 = 51.345 MCells
*  Number of Objects:     95479
*  Objects out of Area:   0
*  Parts   out of Area:   0
*
*  Memory  Estimation  :
*       Main    Field     1175.190 MBytes
*       Overhead          1168.852 MBytes
*
*       pga     Storage    288.820 MBytes (during setup)
*
*                        =========
*                            2.571 GBytes
*
*  Simulation finished Thu Apr 26 21:41:19 2018
*  Simulation time  03:12:55
```

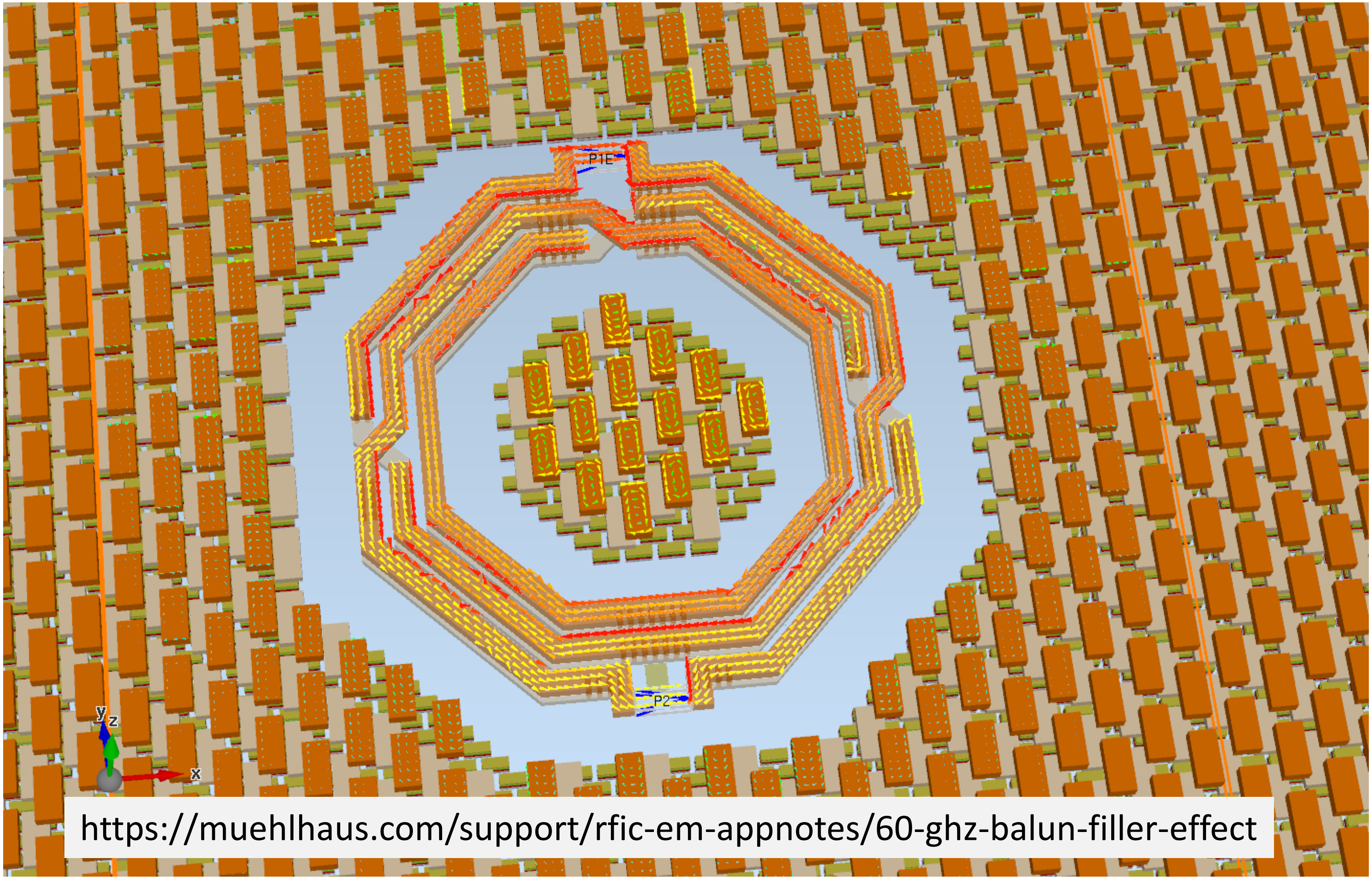
Large Model: Crosstalk Analysis



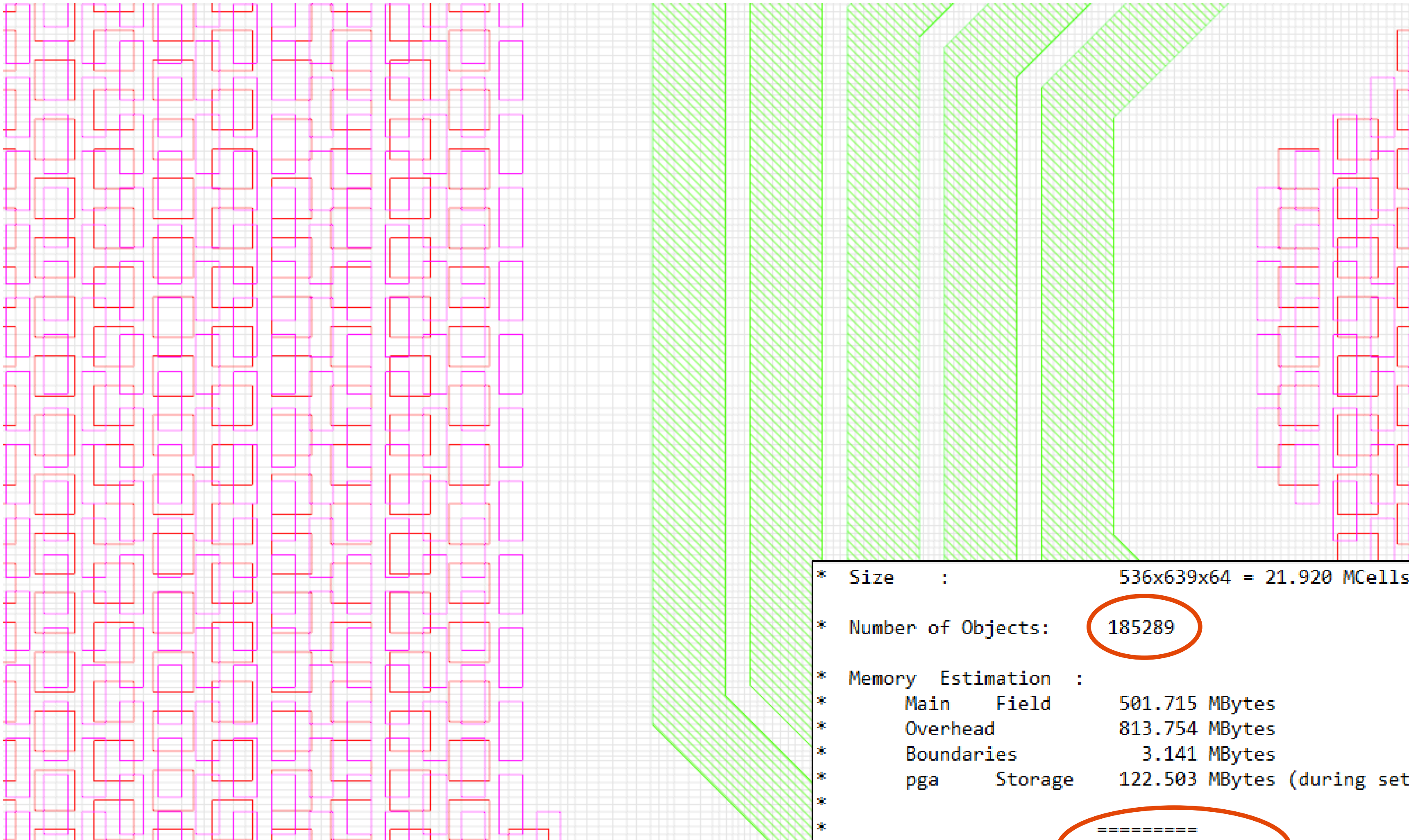

```
*  Using AVX+FMA3 vectorisation Extension in 1 cpu groups, 14 cores alltogether
*
*
*  Geometry w/o abc:       480x446x88
*  Geometry:               482x448x89
*  Size     :              488x450x90 = 19.764 MCells
*  Number of Objects:     51202
*  Objects out of Area:   0
*  Parts   out of Area:   0
*
*  Memory  Estimation  :
*       Main    Field      452.362 MBytes
*       Overhead           321.691 MBytes
*
*       pga     Storage    111.088 MBytes (during setup)
*
*                        =========
*                          885.142 MBytes
*
```

```
*      STEP 265064, 5.62E-03 SECONDS EACH, 3418.566 MCELLS/
*         ENERGY ESTIMATE E 1.181369106373321E-01, H 1.1813
*
*     energy decrement E 51.21 dB, H 51.21 dB.
*
*
*  Collecting Data Tue Jun 05 20:43:16 2018
*
*  Data Collect finished Tue Jun 05 20:43:16 2018
*
*
*  Simulation finished Tue Jun 05 20:43:16 2018
*
*  Simulation time  26:21
*
```

Complex Model: Influence of Filler Metal

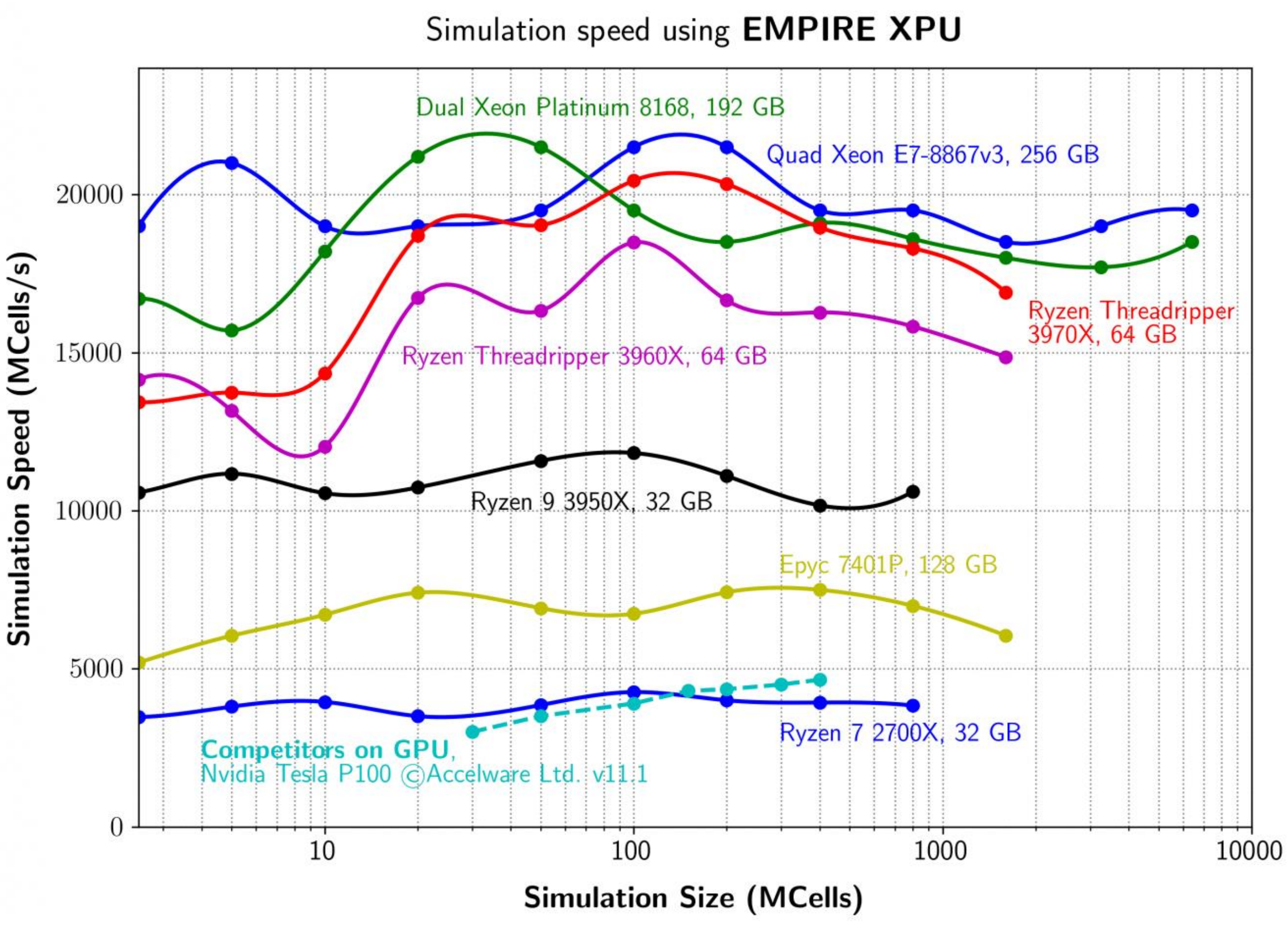


Influence of Filler Metal



```
*  Size     :          536x639x64 = 21.920 MCells
*  Number of Objects:   185289
*  Memory  Estimation   :
*       Main    Field      501.715 MBytes
*       Overhead           813.754 MBytes
*       Boundaries           3.141 MBytes
*       pga     Storage    122.503 MBytes (during setup)
*
*                         =========
*                          1441.112 MBytes
*
*  Simulation finished Mon Apr 02 13:08:07 2018
*  Simulation time   01:11:55
```

Empire Speed (FDTD Cells per Second)



Why is Empire so fast?

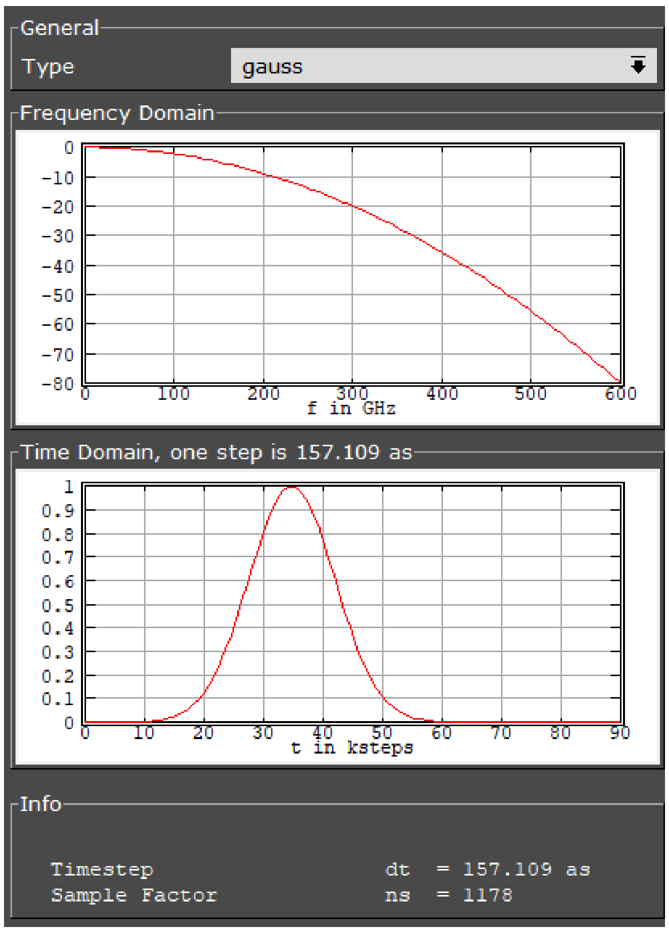
Numerical techniques:

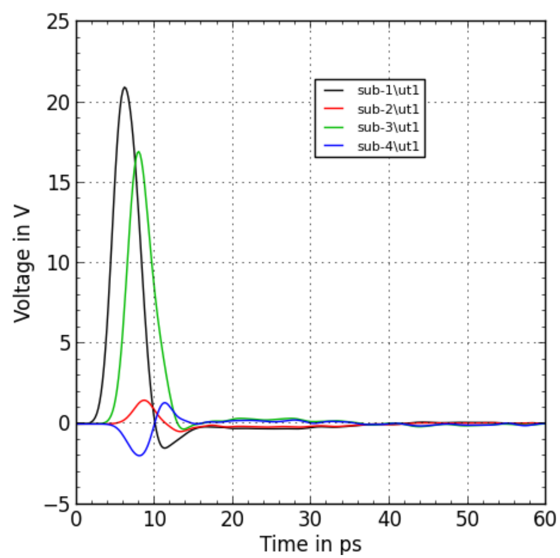
- ✓ Specific C- & assembler-code created "on-the-fly" for each simulation to fit CPU architecture and simulation model
- ✓ Individual code adaptation for latest CPU's (AVX, AVX2,...)
- ✓ Efficient caching & compression of FDTD coefficients
- ✓ Speed not limited by RAM access time due to efficient last level cache usage (multiple time step principle)
  - **XPU-technique** calculates the updates for the E- and H-fields combined
  - multiple time steps of the fields calculated in the cache memory of every core of the CPU

- ✓ **No** Simulation **speed limitation** due to RAM data transfer
- ✓ Efficient multi core usage **possible**

FDTD Method

- ✓ Time domain method, excitation with gaussian pulse
- ✓ Wideband S-Parameter obtained by Fourier transform of time signals at port(s)
- ✓ We get one column of S-matrix (wideband) per port excitation

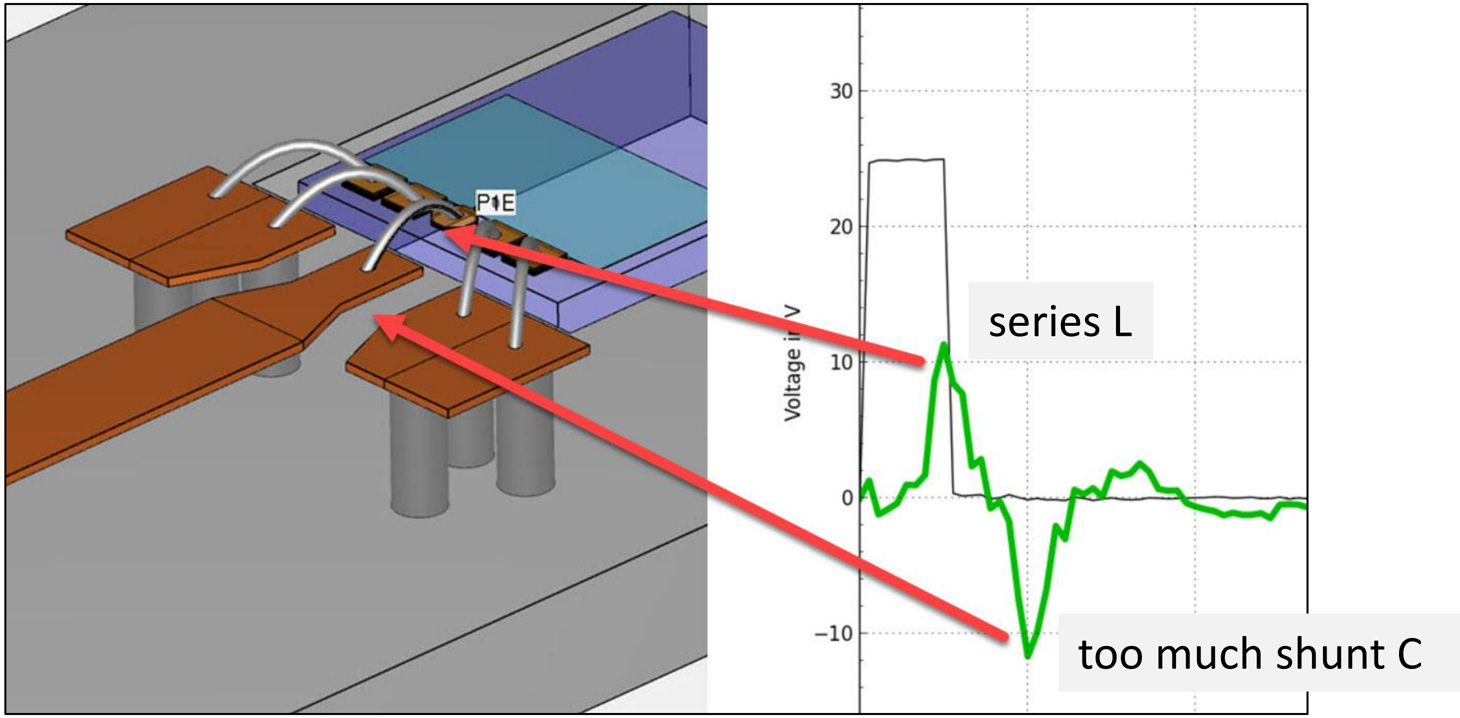




$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{21} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{24} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

Use time domain results instead of S-params

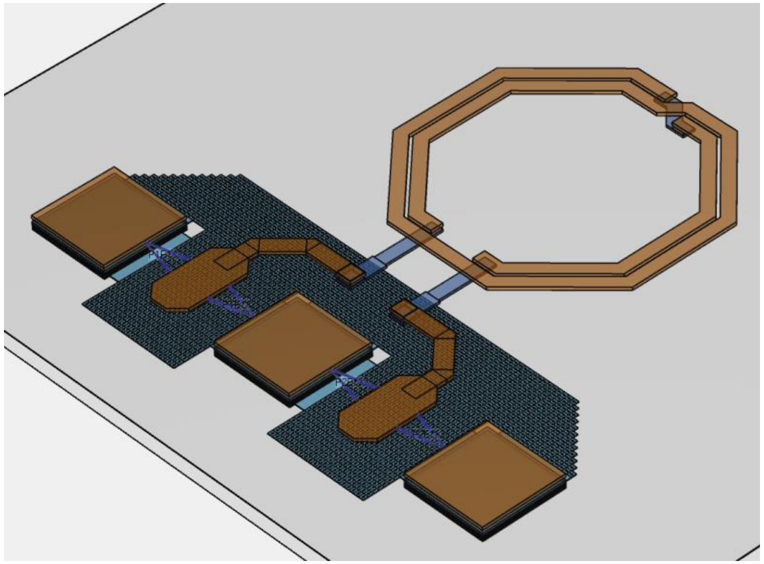
- ✓ Direct evaluation of **time domain pulses** (TDR) is easily possible, to localize discontinuities and help optimizing the signal path
- ✓ Appnote: muehlhaus.com/support/empire-appnotes/rfic-pcb-tdr



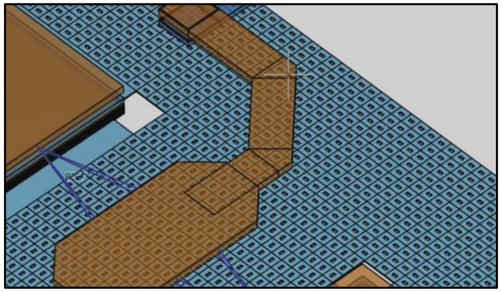
SIMULATION ACCURACY

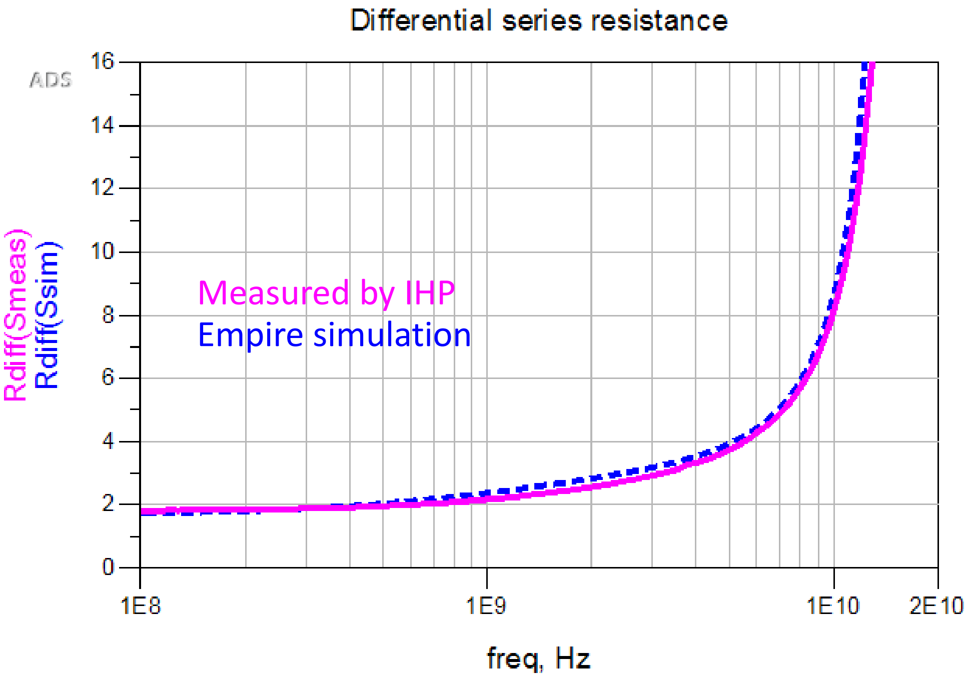
Accuracy: Wideband Loss Modelling

- ✓ Testcase: RFIC inductor with pads in IHP SG13S technology
- ✓ Dielectric model: wideband lossy
- ✓ Metal model: wideband lossy
- ✓ Mesh: 8.7MCells, TopMetal2 mesh hint: max 5µm



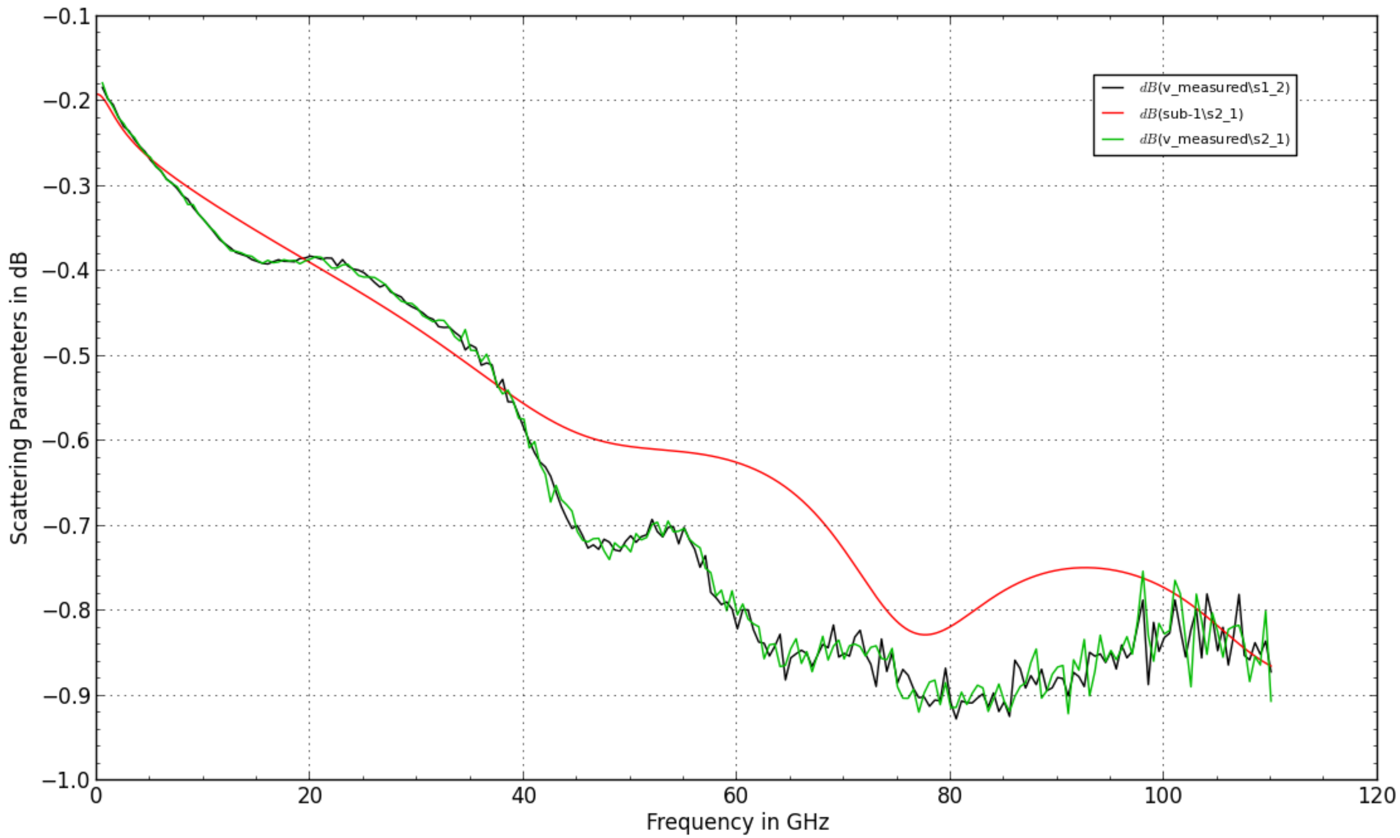
Detail view:



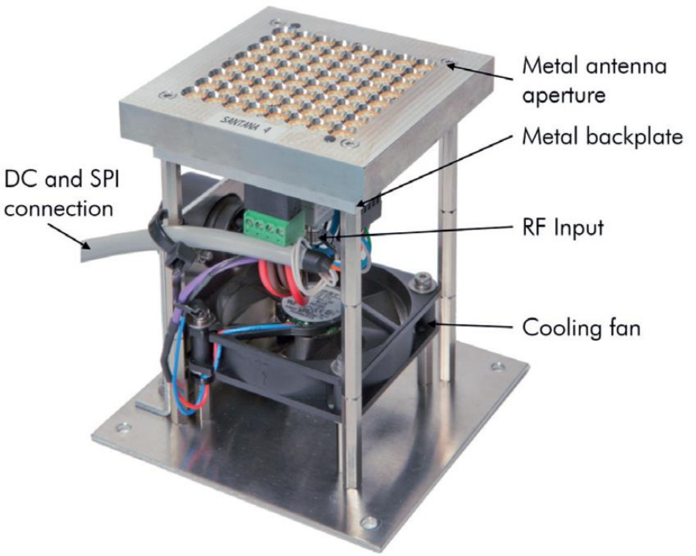


Accuracy: Transmission Line Loss

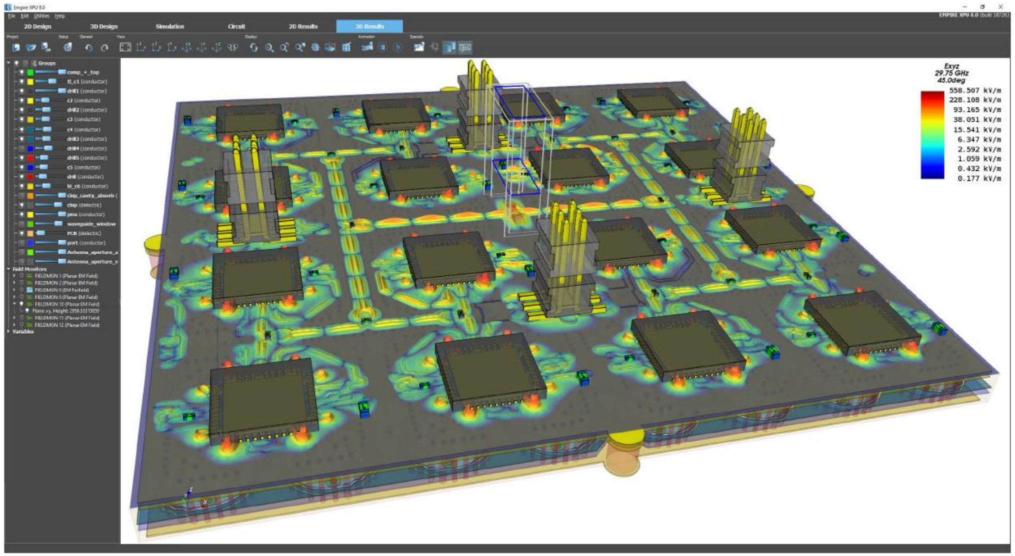
- Testcase: 1080µm transmission line, 15µm wide TM2 over Metal1, IHP measurement de-embedded
- Better agreement to measurement than other widely used EM solvers



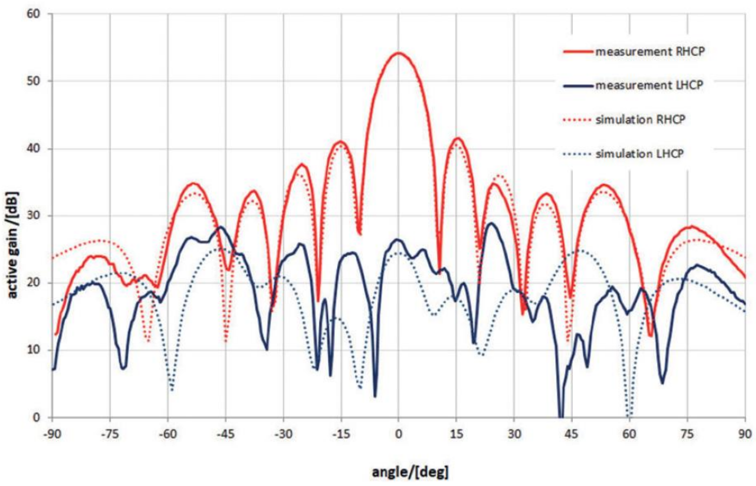
APPLICATION EXAMPLE:
SATCOM / 5G Digital
Beamforming frontend module



Frequency: 20 - 35 GHz
Size: 600 Million cells
Memory usage: 16 GB
Simulation time: < 2 h
Dual Xeon workstation

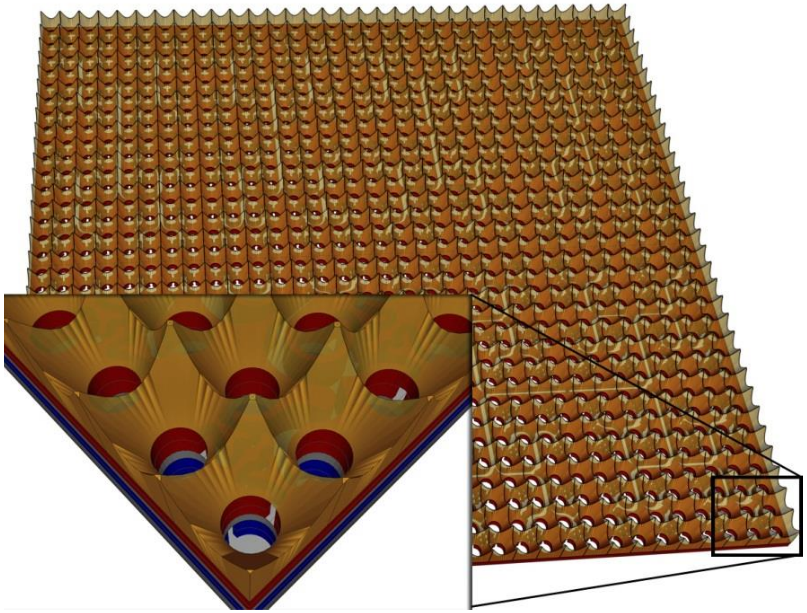


Electric field at chip feed network and antenna feed

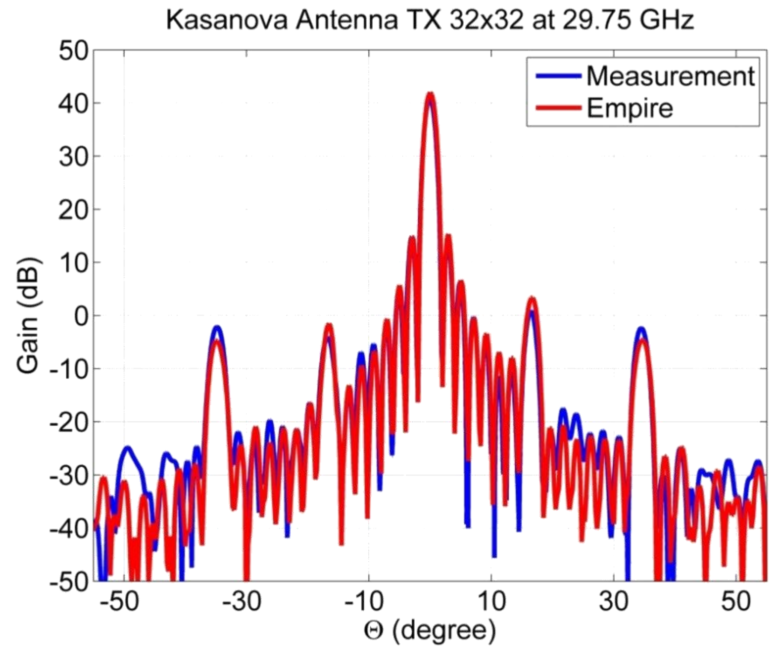


Antenna Farfield pattern simulation vs. measurement

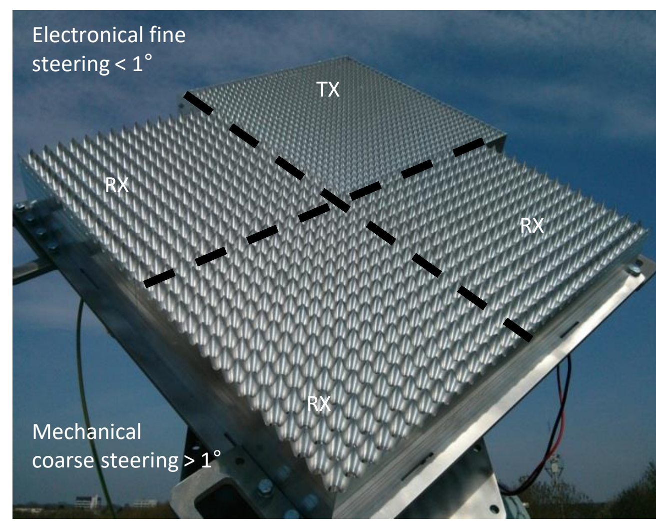
Ka Band Tx Antenna 32x32 Elements



EMPIRE simulation model
32x32 Tx-Antenna

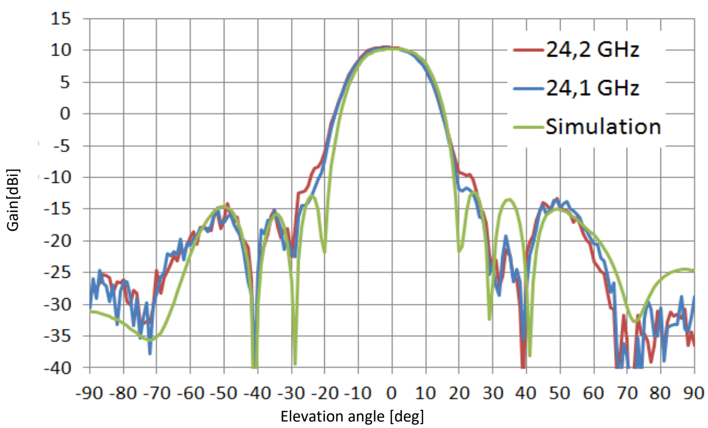


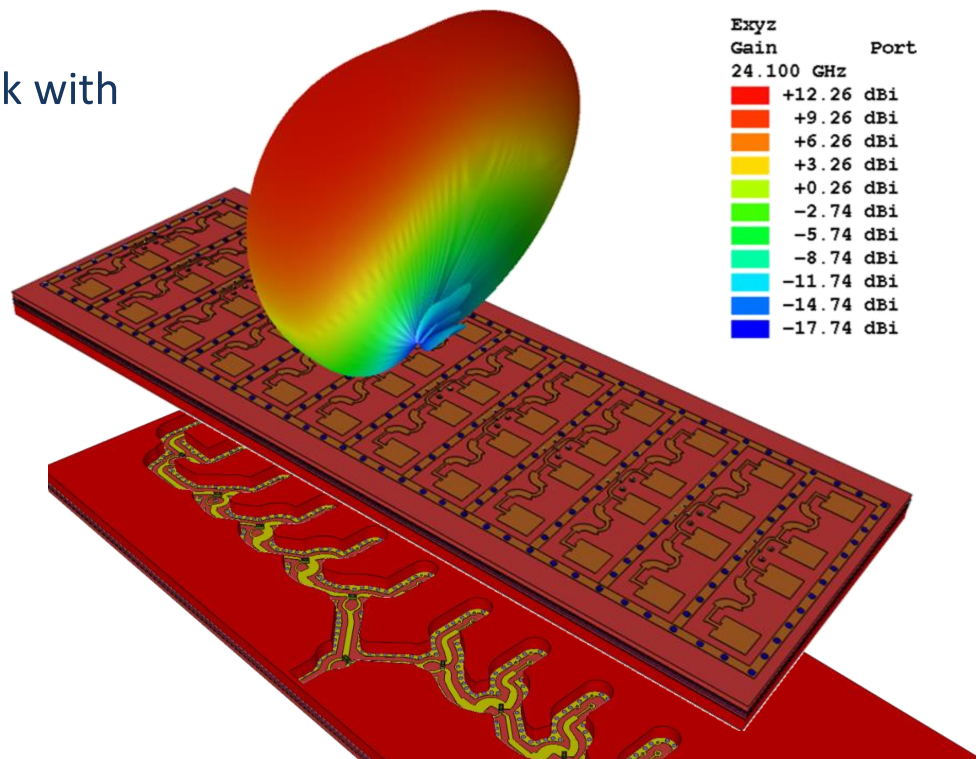
Frequency: 30 GHz
Size: 87 Million cells
Memory: ~ 3.6 GB
Simulation time: 8 min

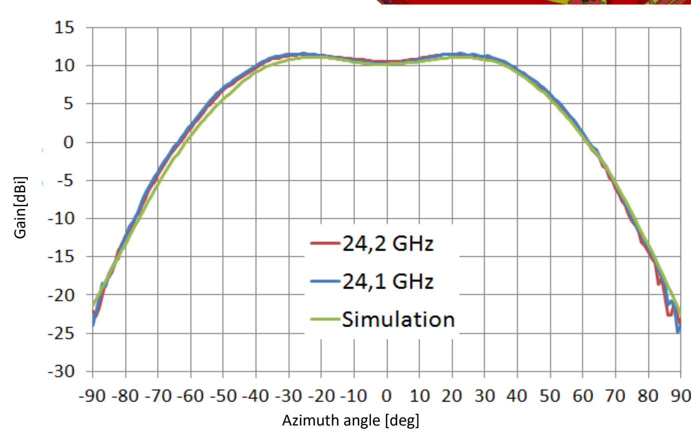


24 GHz radar antenna (TX)

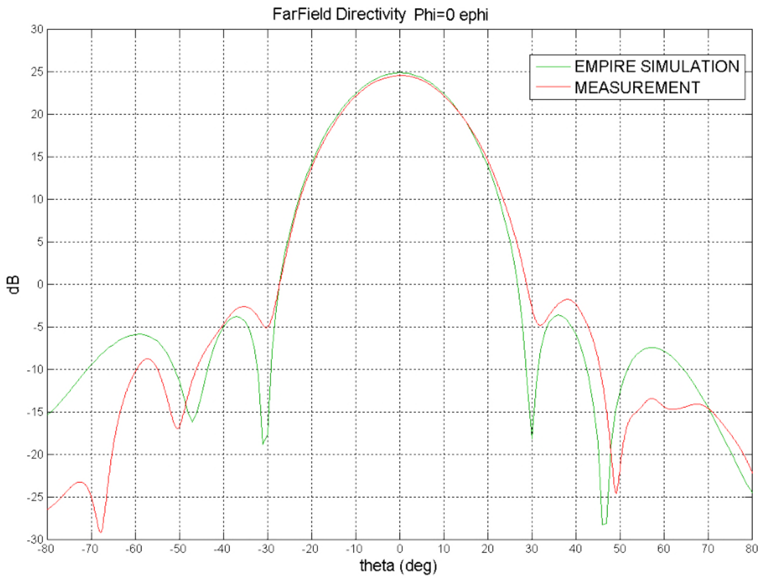
- 4 x 12 element array
- Backside microstrip feed network with Wilkinson dividers
- Accurate 3D EM simulation of antenna, feed network and backside casing

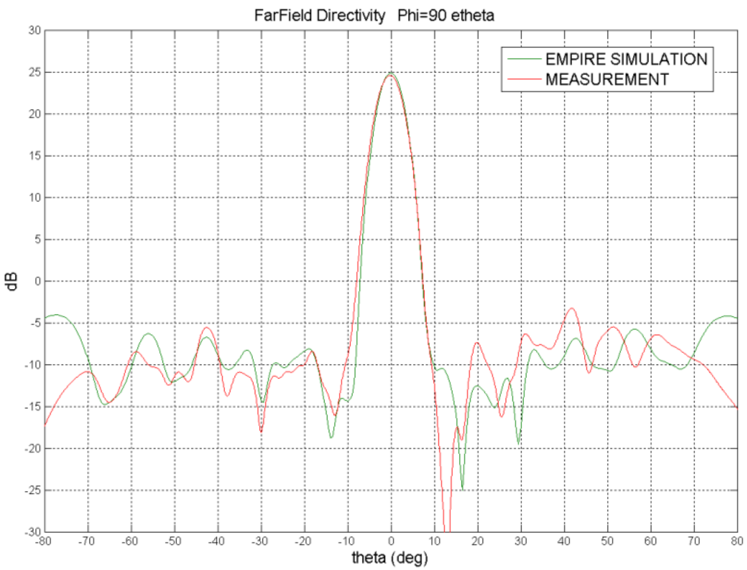




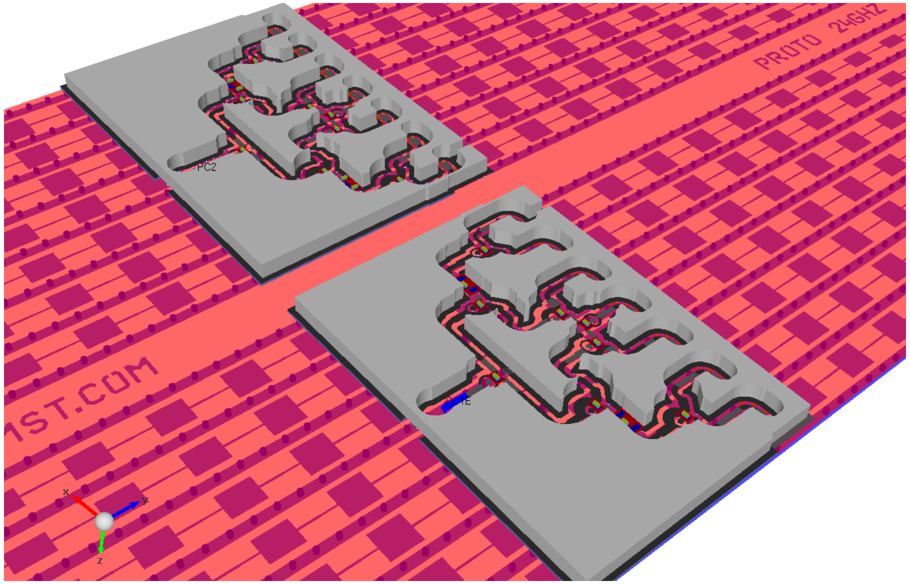


24 GHz Automative Radar Antenna



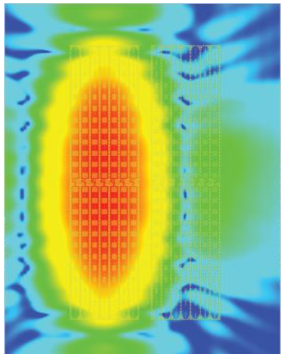


Backside feed network with housing

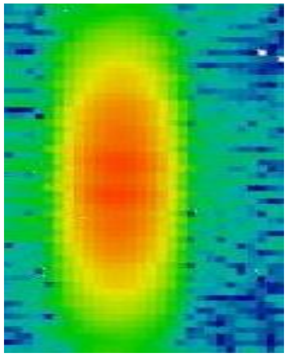


Nearfield – comparison simulation/measurement

simulation



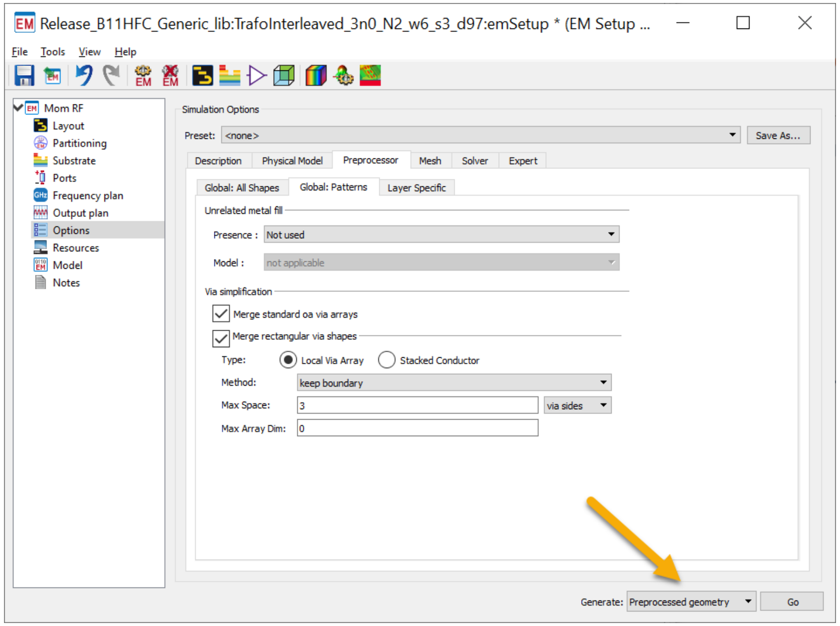
measurement



Layouts from GDSII or ADS

- ✓ Empire can import GDSII, but does not evaluate the purpose
- ✓ You need to use a layer mapping for Cadence export that only exports the actual metal. Do not export fillers, nofill, noDRC or similar purpose!

- ✓ For layout export from Momentum, you can use EM preprocessing to simplify the layout, do via merging and remove purpose like nofill. This creates another (preprocessed) layout view that you can use for GDSII export to Empire.



Stackup/Substrate/Technology

- ✓ Empire stackups (empty projects) available for IHP technologies and IFX B11HFC
- ✓ For other technologies, we have an Empire Script that reads Momentum substrate file and creates an Empire project with all these layer definitions
- ✓ Please contact volker@muehlhaus.com

Empire XPU Summary

- ✓ XPU FDTD solver can handle **very large, complex models**
- ✓ **Much faster** than other time domain solvers by using XPU technology
- ✓ **User interface designed for combined planar + 3D layouts**:
  - ✓ Easily import & edit layer-based planar layout in 2D editor
  - ✓ Switch between 2D editor and full-featured 3D editor at any time
- ✓ **Efficient modelling using technology template and "layers"** that provide z-position, materials, priorities, layer-specific mesh settings and much more.
- ✓ Empire **Templates for SG13, SG25H and SGB25** available from IHP DK server
- ✓ **High simulation speed enables more detailed, more accurate models**
- ✓ Biggest speed advantage seen for electrically large models with few ports

App Notes

- ✓ Understand and control the mesh:
  https://muehlhaus.com/support/empire-appnotes/empire-mesh
- ✓ IHP SG13 Template:
  https://muehlhaus.com/support/empire-appnotes/empire-sg13-template
- ✓ 165 GHz Antenna in SG13S:
  https://muehlhaus.com/support/empire-appnotes/empire-on-chip-antenna-240ghz
- ✓ Time domain for chip-package transition:
  https://muehlhaus.com/support/empire-appnotes/rfic-pcb-tdr
- ✓ Choosing computer hardware for Empire XPU:
  https://muehlhaus.com/support/empire-appnotes/hardware

Most of these appnotes are written for the old Empire 7 user interface, but the settings can also be found in Empire 8

EMPIRE XPU MODULES & PACKAGES

PACKAGES / MODULES	3D EDITOR	SIMULATION CONTROL	XPU FDTD SOLVER	FAR FIELD TRANSFORMATION	TE/TM WAVEGUIDE MODES	SAR AND VOXEL EDITOR	OPTIMIZER	CIRCUIT SIMULATION	CLUSTER SOLVER	THERMAL SOLVER	VOXEL POSER	CAD EXCHANGE: 2D LAYOUT RW *	STL RW	ODB ++ R	ACIS RW	IGES RW	STEP RW	NX R	DXF R	INVENTOR R	PARASOLID R	PRO/E R	SOLIDWORKS R	SOLID EDGE R	CATIA 4 RW	CATIA 5 RW	JT R	VDA RW
PLATINUM	X	X	X	X	X	X	X	X	X			X	X		X													
BIO	X	X	X	X		X				X	X	X	X		X													
GOLD	X	X	X	X	X	X	X	X				X	X		X													
SILVER	X	X	X									X	X															

CAD EXCHANGE

R=READ

W=WRITE

* includes GDSII import/export

About Empire XPU

Empire XPU is a product of IMST GmbH
founded 1992
engineering staff: 180 employees, 130 engineers / PhD

Contact for Empire @ RFIC: Volker Mühlhaus
Dr. Mühlhaus Consulting & Software GmbH

volker@muehlhaus.com
www.muehlhaus.com

https://muehlhaus.com/products/empire-3d-em
https://muehlhaus.com/support/empire-appnotes