RFIC Stacked Metal in Sonnet Inductor Models

Purpose of this document:

The purpose of this document is to assist you with simulation of inductors that have stacked metal, connected by vias. Often, these vias cover the entire conductor area, making the analysis slow and take much memory. We will investigate better modelling techniques that are more efficient in terms of simulation time and memory.

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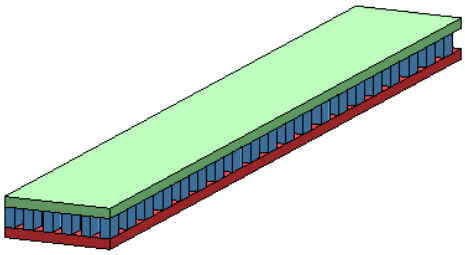
1. Introduction

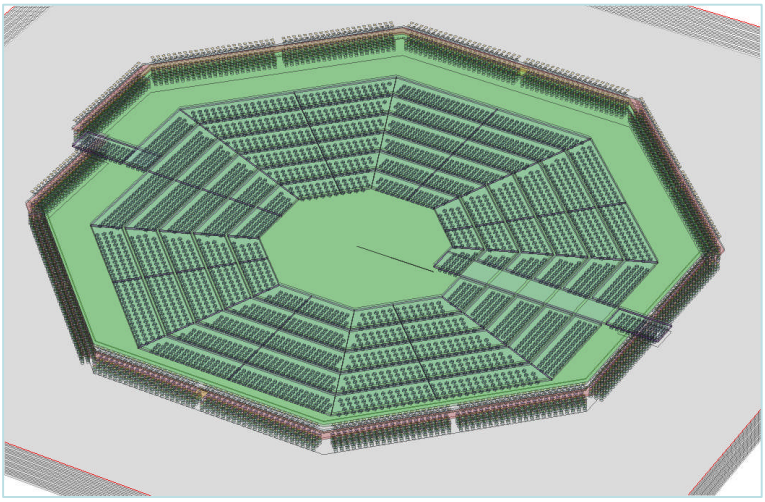
The purpose of this document is to assist you with the simulation of inductors that have stacked metal, connected by large via arrays.

In RF optimized technologies, we usually have at least one thick top metal layer that can be used for inductors. But in small technology nodes, all available metal is quite thin and the conductor series resistance is limiting the maximum Q factor for inductors in the frequency range up to 5GHz or so.

To overcome that problem, multiple metal levels can be connected in parallel, for an increased cross section and reduced series resistance.



Often, these via arrays cover the entire conductor area, making the analysis slow and taking very much memory.



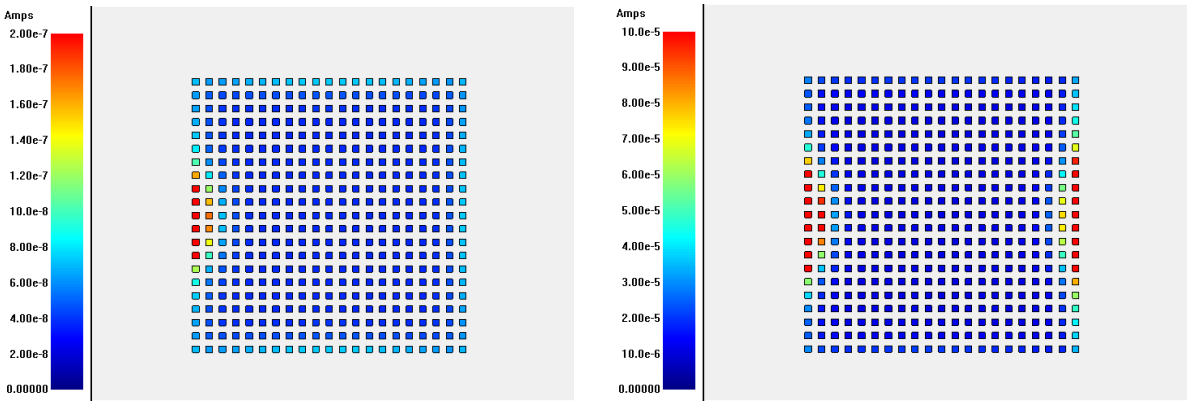
We will investigate modelling techniques that address this problem, to reduce simulation time and memory requirement. These techniques are based on the analysis via array behaviour at RF frequencies, which leads to possible via simplification.

2. Why can we simplify?

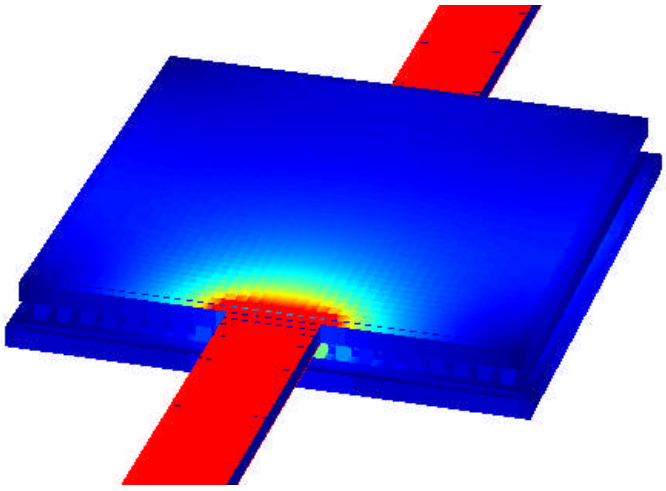
The reason why we can simplify the model is that some vias have much less current (and thus much less effect on the result) than other vias, depending on their location.

It is well known that for high frequency, skin effect pushes the current to the edges of a conductor. Something similar happens if we have large via arrays: the current is highest at the edges, and there is only very small current in the middle. The higher the frequency, the stronger this effect is.

Below is a plot of the current through the via array in a MIM capacitor, at 10 MHz (left) and 50 GHz (right). Red indicates high current and dark blue indicates no current. You can see that the current changes layer through the vias near the edges, and the inner vias have no effect. Even at frequencies as low as 10 MHz, the current is mostly at the edges, and there is very little current inside.



Here is the 3D current view of the same structure, where you can see the feedlines.



The topic of this application note is inductors, not MIM, but we can learn something useful from these pictures: the vias in an array are not of equal importance. The edge vias are most important, whereas the inner vias have only small RF current. This means that we can selectively remove vias, with very little change in results.

3. Inductors with stacked metal

In an ideal world, we would build inductors from a really thick top metal (=low series resistance) that is far above the substrate (minimized coupling to the lossy substrate).

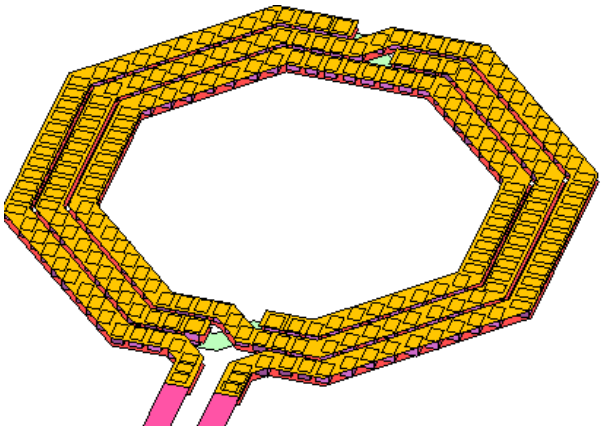
Unfortunately, in some technologies, all available metal is quite thin and the series resistance is limiting the maximum Q factor. To overcome that problem, multiple metal levels can be connected in parallel, for an increased cross section and reduced series resistance.

The typical case is that metals are connected with a large array of "normal" vias, which allow vertical current between the metals. These vias do not provide additional cross section for the inductor current, they only connect the parallel conductors and allow the inductor current to equilibrate between the parallel conductors.

As we have seen in the MIM example, some vias are more important to the high frequency current than others, depending on their location. This also applies to inductors with stacked metal.

We will study this with an example case, where two parallel conductors are connected with many small vias. The feedline is connected at one level only, so that the current has to change layers at the feed, and at the underpasses.

The baseline analysis, which we consider accurate but inefficient (slow, much memory), is that we include all these vias in the simulation model. Later, we will check more efficient models against this baseline.



top view

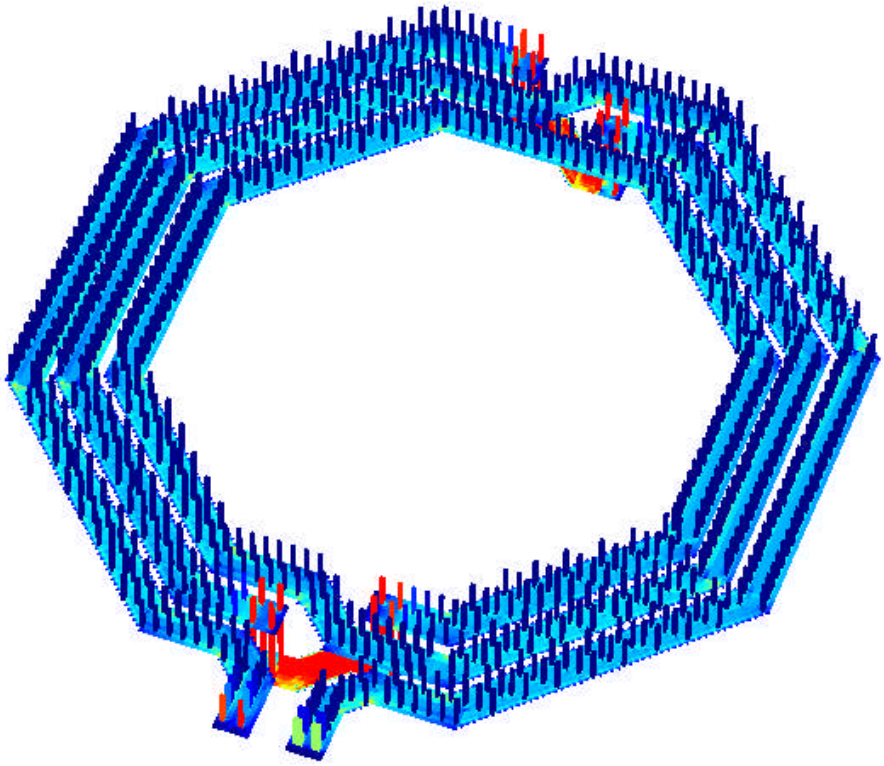
Note that this baseline will take long simulation time and much memory for **two** reasons:

- The vias will cause additional subsections near each via, and
- the Sonnet meshing will revert from conformal to staircase near vias.

The presence of the vias everywhere means that conformal mesh can not be used, and any polygon where we assign conformal mesh will automatically revert back to staircase, This is a big disadvantage because conformal mesh is much more efficient for diagonal lines than staircase.

But let's talk about results now.

The image below shows the via current for that inductor with two metal levels connected in parallel. The upper metal is hidden in this plot, so that we can see the via currents.
The z-axis is stretched for easier visibility. Frequency is 0.1 GHz.



Red indicates high current and dark blue indicates no current. As you can see, even at this low frequency of 0.1 GHz, the current flows mostly through the vias at the "end" of the line, where the current has to split to the parallel conductors. In between, there is very small current. Once the current has split onto the parallel conductors, it just keeps flowing in parallel, without changing the layer, until it reaches the vias at the end of the parallel line.

At higher frequencies, we see a similar behaviour.

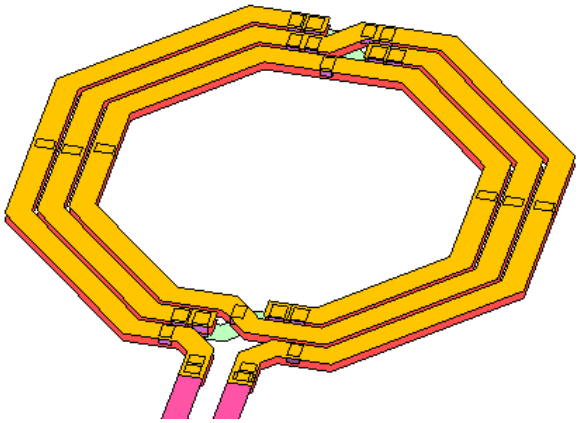
The message is simple:
Most of the vias have no effect on high frequency results.
They will slow down the analysis, but don't change results.

From this, we can derive a strategy for more efficient simulation.

4. Selective removal of vias

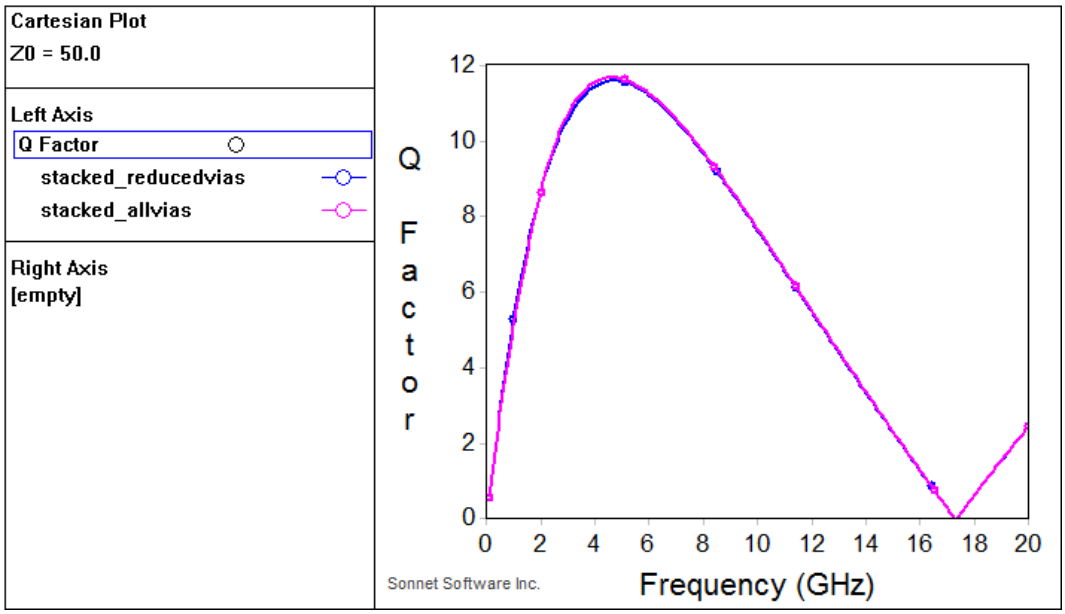
If some vias don't change results, we can delete them from the model. This will allow us to use efficient conformal mesh for large parts of the layout, because now the vias are only in selected places.

In this example, we have deleted most of the vias, and only kept the vias near the end of the parallel conductors, where current must change layers. The properties of these remaining vias are unchanged.



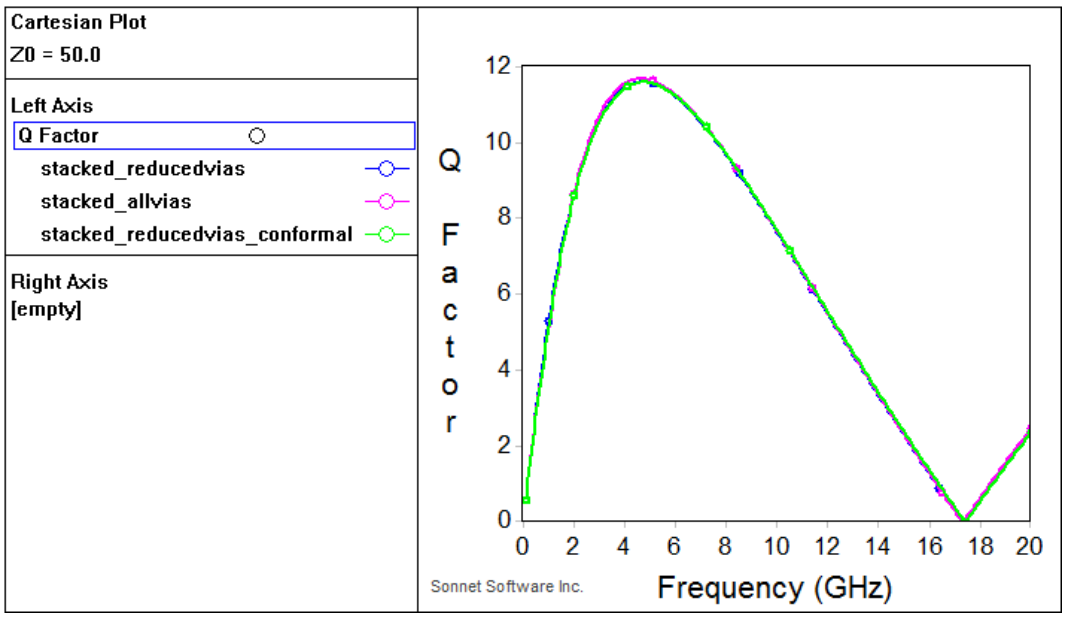
The reason for not changing the via properties is that the current will "see" the true physical via properties in those places where current flows, and we should not try to combine the total cross section of the entire big via array into some effective properties for the remaining vias. Don't worry if this thought is confusing here - we will come back to this later when we discuss Sonnet via merging and via meshing.

The plot below shows the comparison of Q factor between the baseline model, with all vias, and this simplified model shown above, where most vias have been removed.



As you can see, results are very similar. Deleting all the vias in the middle of the line has not changed results.

To make sure that the above model with reduced vias is not affected by possible small differences between conformal mesh and staircase mesh, it was simulated with staircase mesh, just like the baseline model with all vias. A big improvement in simulation speed and required memory is seen if we now use conformal mesh. Below, that conformal mesh result is added to the comparison. As you can see, they are almost identical.



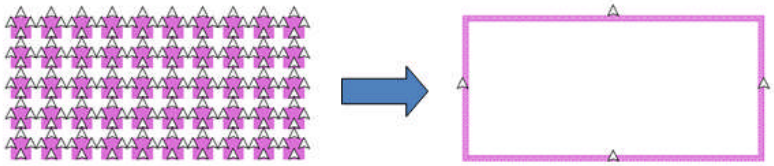
Here is a summary of the simulation time and required memory:

	Time per freq.	Memory
Baseline with all vias	37 min	7495 MB
Reduced vias, staircase mesh	13 min	4262 MB
Reduced vias, conformal mesh	4 min	1915 MB

How to apply this to your real cases?

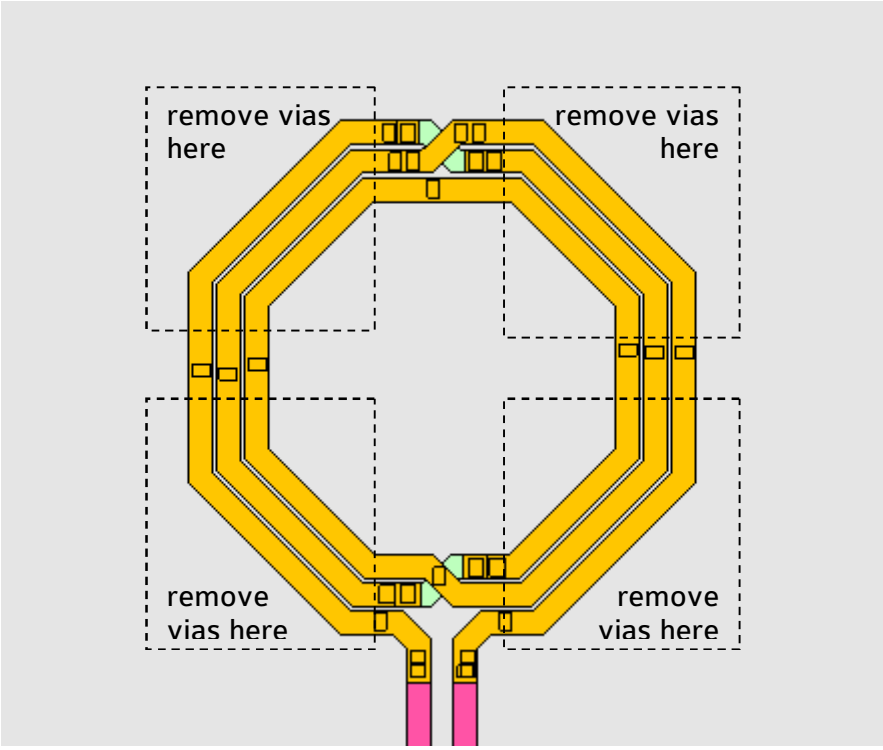
In your real technology, there will be even more and even smaller vias than in this example. We did not show that because the example with all vias already needed 7.5GB of memory. We simply could not simulate the baseline with even more vias.

In your real technology, we suggest a combination of **manually deleting obsolete vias**, and automatic **merging for the remaining, relevant vias**.



When you create the **Sonnet EM view** in Cadence, this still includes all vias, similar to the layout view. Now the first step is to modify the Sonnet EM view and delete the areas where vias are not needed, as shown below.

For the remaining vias, you can use the automatic via merging as implemented in the Sonnet Cadence interface, to make these required vias simulation friendly.[1]



[1] For the mesh setting of these merged vias, we recommend the default "ring" meshing, so that current can flow on all sides of the merged via.

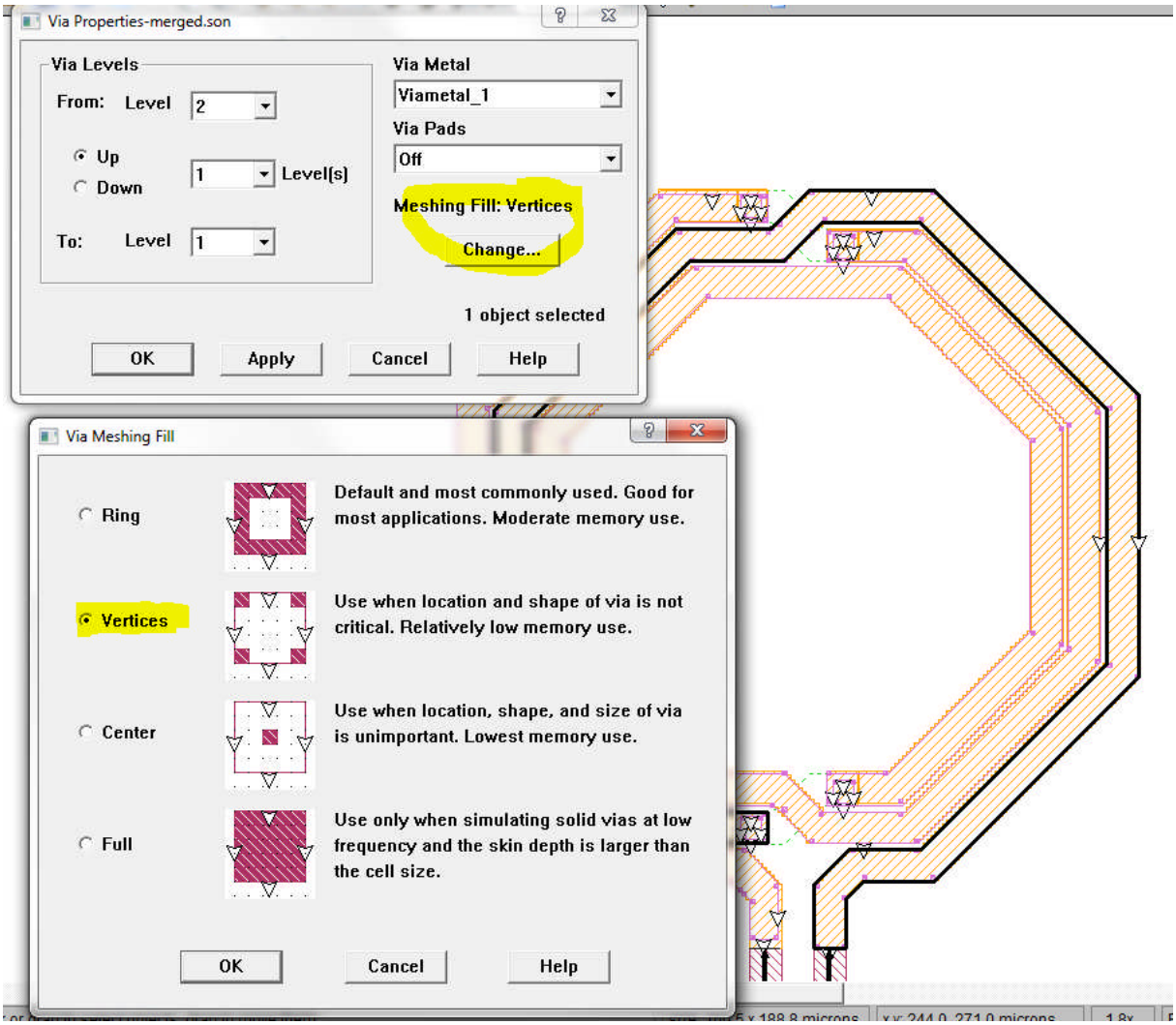
5. Alternative approach: Via merging plus vertices via meshing

With Sonnet 13, there is an alternative approach that takes advantage of the new via meshing setting. The simulation will not be as efficient as for the manual via removal discussed in chapter 4, but the advantage is that it can be fully automated.

This alternative approach is based on via meshing with the "Vertices" setting, which will place via subsections only in the edges of the via polygon.

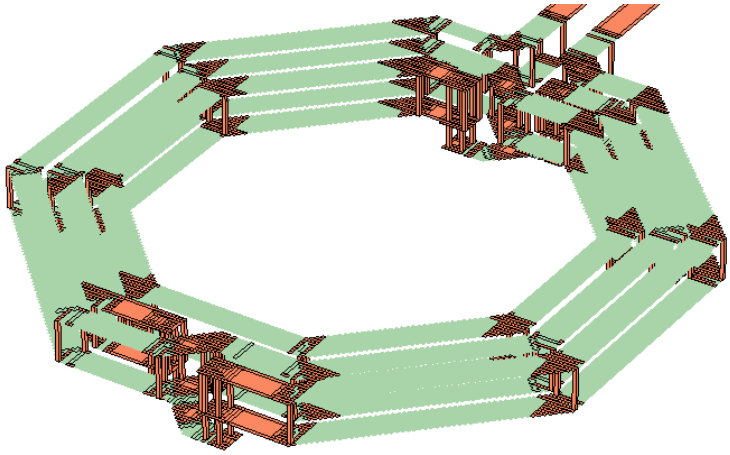
First, by using via merging, we make sure that Sonnet creates big, merged via polygons for the entire area, which follow the conductors above and below. Even if the via array does not match the boundary of the conductors exactly, the Sonnet via merging algorithm will adjust the merged via polygon to be aligned with the conductor boundary. It will also calculate the new via metal properties, so that the merged via will have the same DC (!) resistance as the array.

Now that we have the big merged via polygons, we can use "Vertices" via meshing, instead of the "Ring" default. This via meshing can be configured in the Cadence interface on a per-layer basis, or manually in the xgeom editor for each via.



The effect is that the number of via subsections is reduced, and that they are only in a few places. With via subsections only in a few places, conformal mesh can be used in large parts of the model.

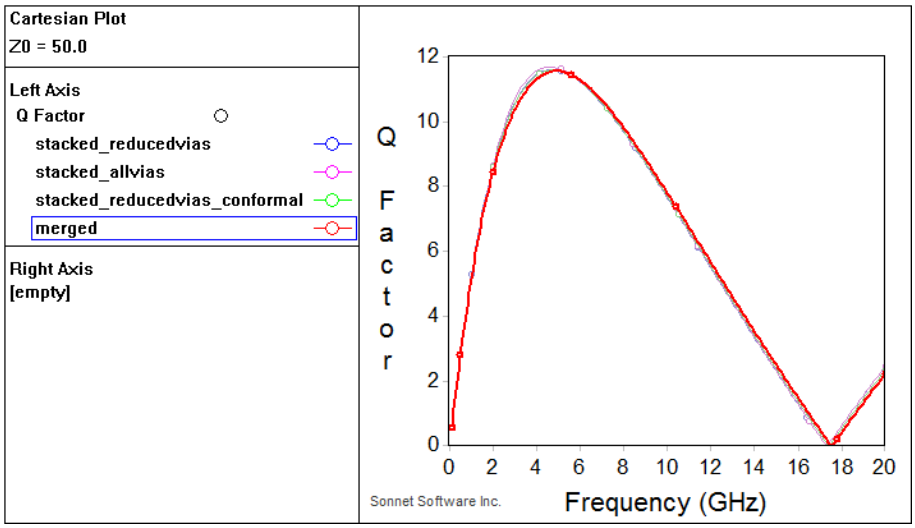
Below is the subsection view for that case, showing how the big via polygon is now represented by a few selected via subsections in the edges.



Conformal mesh is kept intact for most of the model, and automatically reverts to staircase only near the via subsections[2].

One concern with this approach is that via merging and via meshing both tweak the via properties, to keep the total DC resistance unchanged. However, we have seen that the current will flow only in some vias at the end of the line, and most vias have no effect on the RF resistance. Now if the algorithm takes the entire via cross section, based on DC calculation, and tweaks the via subsections to have the same total DC resistance, it might move via cross section from a "no current" part in the middle of a line to the end of the line, changing the effective RF resistance.

However, in this actual example the results agree well with all the previous results.



[2] At least, we hope it does. In some cases, the algorithm might switch a larger layout segment to staircase which is not really needed. The Sonnet programmers are working on the algorithm for this case, to make it better for future versions.

For suggestions and questions related to this document, please contact:
Volker Mühlhaus, volker@muehlhaus.com