

Defining a stackup for Sonnet RFIC analysis

Purpose of this document:

The purpose of this document is to assist you in defining the dielectric layers and metal definitions for Sonnet, based on the technology cross section provided by the semiconductor foundry. The side effects of thick metal vs. thin metal stackup are discussed.

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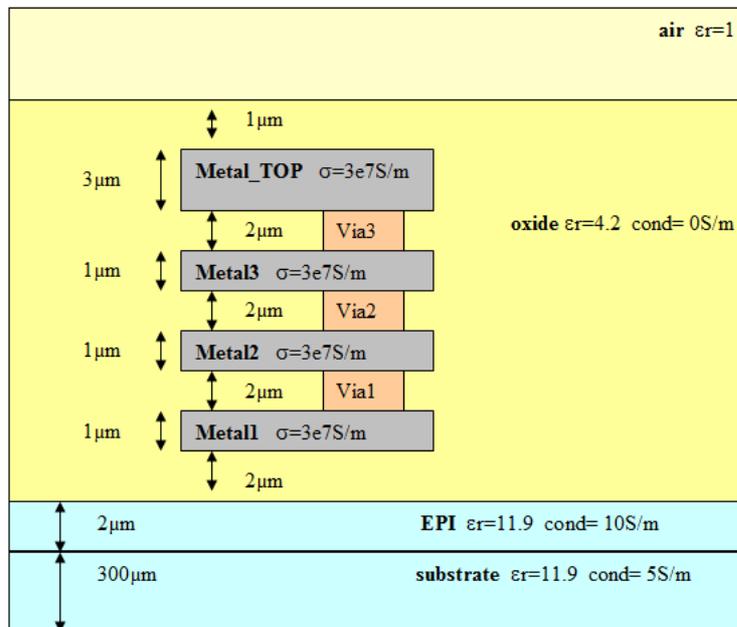
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Document revised: 18. August 2011

Document revision: 1.1

Simple example technology

In this document, we will use a very simple example technology to explain the corresponding material definitions in Sonnet. The back end cross section of that example technology is shown below.



Conductors

The example technology has three conductors of 1µm thickness and one top conductor of 3µm thickness.

In the foundry's data sheet, conductors are usually defined with conductor thickness and the Ω/square DC resistance. The required data in Sonnet is conductor thickness and conductivity¹. The equation to calculate the conductivity σ from the data sheet values is:

$$\sigma = \frac{1}{RDC * t}$$

where RDC is the Ω/square DC resistance and t is the conductor thickness (unit m).

Reference values: Conductivity of pure aluminium is 3.72e7 S/m, conductivity of pure copper is 5.8e7 S/m.

Vias

In Sonnet 13, a new via loss model has been introduced, which takes the actual simulated cross section into account, and keeps the correct DC resistance even if the vias are merged into big blocks that are more efficient for simulation.

¹ There is a Ω/square metal model in Sonnet, but this is designed for resistors and sets that exact value for all frequencies, without modelling skin effect.

In Sonnet 12 and before, the via losses were somewhat complicated to set, because the vias were simulated as hollow tubes, with a metal surface impedance mapped to the via side walls. Also, exact via loss modelling depends on the cross section of the via in simulation (hollow tube of merged vias or many individual vias).

In many cases, the vias contribute only a small fraction to the total circuit resistance, so that an exact definition of the via losses is not required. You could simply use lossless metal for vias, or set a physically meaningful conductivity for the materials used. Note that the "thickness" parameter for via metal in Sonnet 12 and before is the wall thickness of the via side walls, and not the vertical length of the via. This thickness determines the via resistance at low frequency, where the skin effect has not yet taken over, and the resistance depends on the via cross section (and conductivity, of course).

If your model requires a very accurate modelling of via loss, please check your via metal definition with a test case against known/measured data (there is some via resistance data in the foundry's data sheet) and contact us for detailed instructions on via metal definition.

Dielectric materials

The dielectric materials are defined in the foundry's data sheet.

One detail that needs attention is the thickness of dielectric layers, because this also depends on the modelling of conductors (thick metal vs. thin metal model). This will be explained in detail later in this document.

Substrate

For Sonnet, the substrate is just another lossy dielectric layer. The substrate conductivity is set in the dielectric layer properties. If you have detailed information about the conductivity profile in your substrate, you can include the graded conductivity by splitting the substrate into multiple dielectric layer definitions with different conductivity.

Passivation

The passivation above the top metal is already planarized in this simple example. In a real technology, we would have non-planar passivation, so that the material above and between the top metal conductors is a mixture of different materials. In many cases, the effect of that layer on the simulation results is small², and it is sufficient to model the passivation as a homogeneous planar dielectric. In case of doubt, it is recommended to simulate with two different values: one simulation with the minimum ϵ_r and a second simulation with the maximum ϵ_r from the materials used in the non-planar passivation, to estimate the maximum possible error from our planarized assumption with a single material.

² The dielectric material will change the capacitance between inductor turns, which is in parallel with the conductor-substrate-conductor capacitance. Check the self resonance frequency for possible changes.

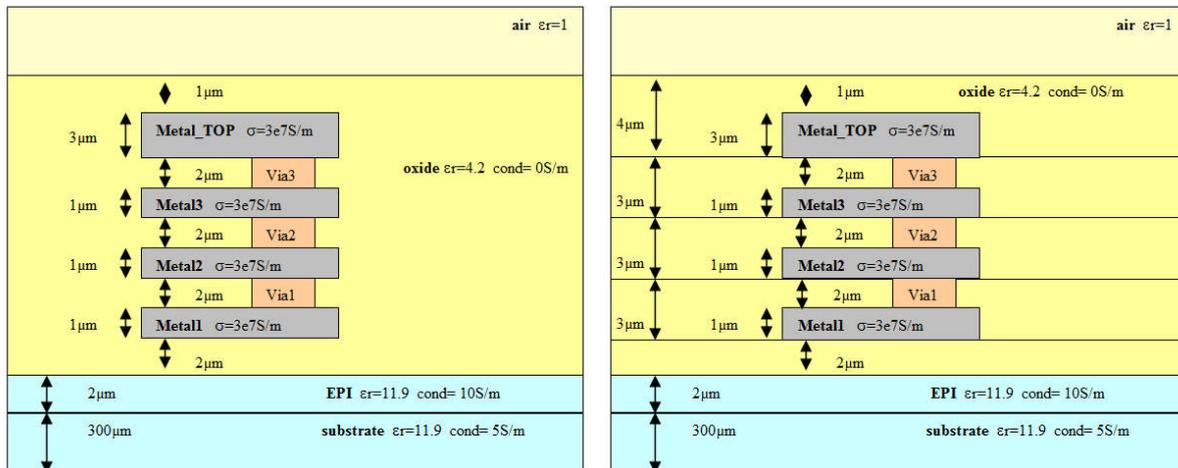
Sonnet thick metal stackup

The most accurate way to model an RFIC technology in Sonnet is to use thick metal models for all metal levels. This ensures that the capacitance between layers and the capacitance from each layer to the lossy substrate is both correct.

When defining the dielectric layer for Sonnet, note that thick metal will penetrate into the dielectric above.

This is different from Agilent's ADS Momentum, where the dielectric thickness will be expanded up or down automatically when a thick metal is used. In Sonnet, there is no automatic expansion of dielectric layers. What you see in the dielectric layer setup is what you get, and a thick conductor will grow into (or even through) the dielectric above.

For our example technology, we can define the oxide layers with a thickness of $3\mu\text{m}$, so that for a metal thickness of $1\mu\text{m}$, we have an effective $2\mu\text{m}$ distance to the metal above.



Hardware stackup

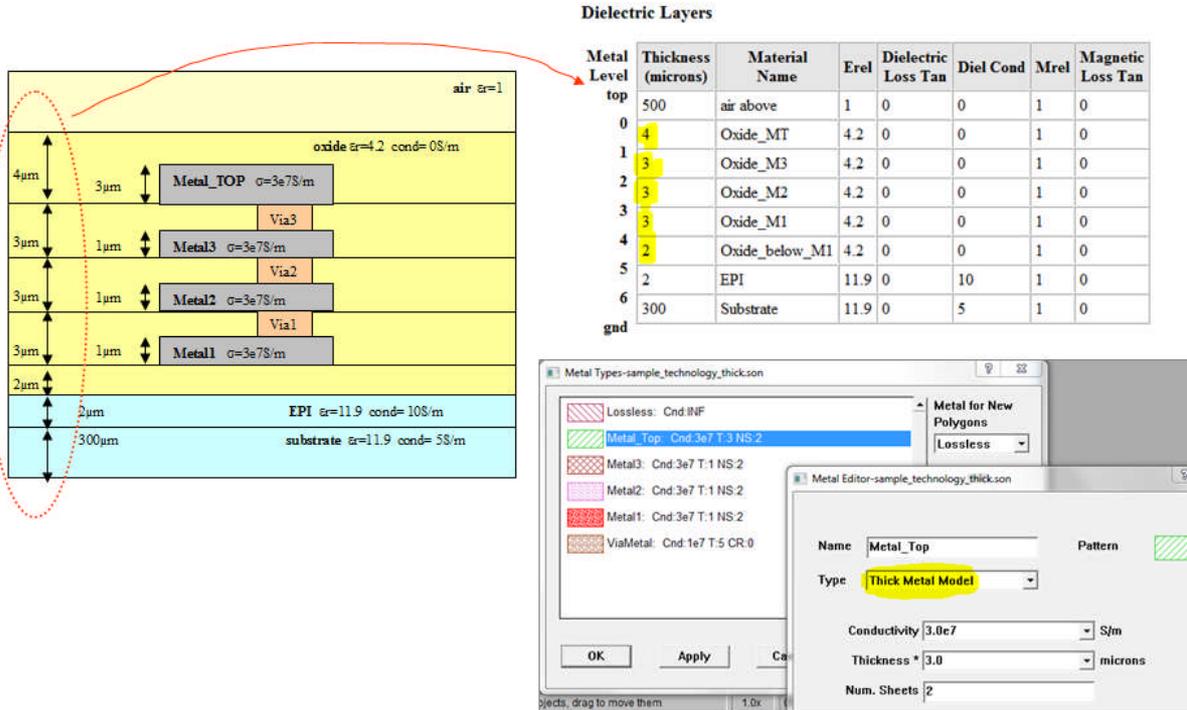
Thick metal stackup for simulation

In this example, there is one dielectric layer definition per metal layer, so that the metal layers in Sonnet are on adjacent Sonnet metal levels. This simplifies the use of the Sonnet editor (one level up/down in Sonnet editor switches to the next RFIC metal layer) and works well with the Sonnet simulation defaults (mesh alignment³ checks one layer above and below).

An alternative thick metal stackup definition could be defined, using one dielectric layer with a height similar to the metal conductor (here: $1\mu\text{m}$ for Metal1-Metal3) and an additional dielectric between the metals (here: $2\mu\text{m}$). This will work, but it has some side effects on usability (metal only on every 2nd Sonnet layer) and the mesh alignment (metal polygons are now two layers apart, so that the default to check layer directly above and below does not find any metal boundaries). For these reasons, the first approach shown above is recommended.

³ Default value for Analysis > Advanced Subsectioning > Polygon Edge Checking is one level.

Thick metal example



For the thick metal definition, leave the default for the number of sheets. This is the best setting for most cases.

Thin metal stackup

In Sonnet, conductors can be modelled with thick metal model or thin metal model ("Normal").

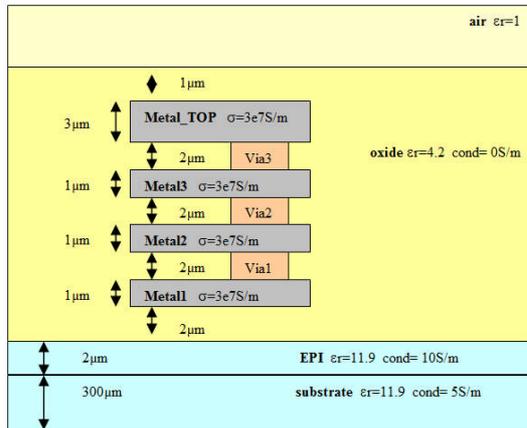
The thin metal model uses a surface impedance mapped onto the surface of the conductors, so that metal loss can be included in the simulation. This is the most memory efficient metal model in Sonnet, because the conductor is internally represented by a single current sheet.

The thick metal model was developed for those cases where the thickness of the conductor changes the field distribution, so that the conductor thickness must be included in the simulation for accurate results. Examples are closely spaced lines where the metal height is on the order of the gap width, or thick narrow lines where the metal height is on the order of the line width. The thick metal model needs more memory for analysis than thin metal ("Normal") because it is internally represented by multiple conductor sheets.

In RFIC technologies, there is another reason to use a thick metal model:

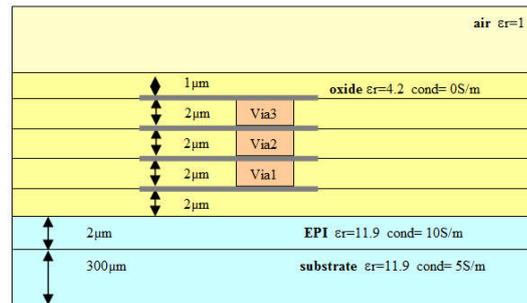
Only with a thick metal model, we can ensure that the capacitance between the conductors and the capacitance to the substrate is both correct. With a thin metal model, it is not possible to create a generic stackup that is always correct in both parameters. This issue will be shown now.

If we define the thin metal stackup so that the dielectric layer thickness between the metals is correct, then the upper metal layers will be too close to the lossy substrate. This is because the metals are simulated with infinitely thin sheets, and for the layers above, the missing metal thickness translates into a reduced distance from the substrate.



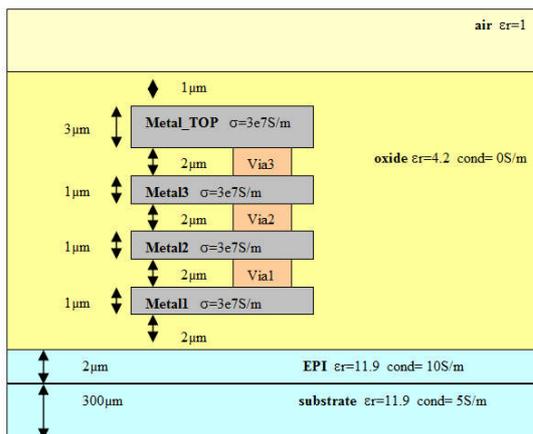
Hardware stackup

Correct for capacitance between metals.
Wrong for capacitance to substrate.



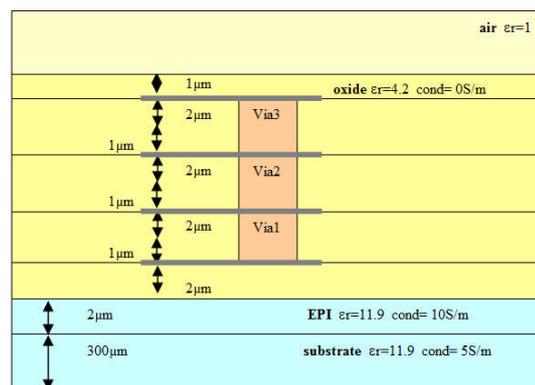
Thin metal stackup for simulation
with 2µm oxide thickness

If we define the thin metal stackup so that the distance from the lossy substrate is correct for all layers, this means that we now have too much distance between the metals, because the metal conductor height is zero in the simulation model (infinitely thin sheet).



Hardware stackup

Wrong for capacitance between metals.
Correct for capacitance to substrate.



Thin metal stackup for simulation
for 3µm (2+1) oxide thickness

Both approaches can be applied to specific applications, if we know what the device under test is and if we know that an error in capacitance to the substrate, or between metals, can be accepted.

Also, a special thin metal stackup can be created that has the correct metal to metal distance, and the correct capacitance to the substrate is obtained by adjusting the dielectric layer thickness below. These special stackup models for specific applications can be used by advanced users, of course, but they are not generic enough to be used for "everything".

Mixed stackup

Often, a mixture of thick and thin metal can be useful, where a large complex ground shield is simulated with thin metal and the inductor above is simulated with thick metal, with appropriate modifications to the dielectric layers so that relevant distances are correct. The author hopes that this document has given you some insight into the side effects and trade off related to thick and thin metal models.

If there are questions or comments, please do not hesitate to contact us:
support@muehlhaus.com